CMS32L032 Datasheet

Low-power 32-bit microcontrollers based on ARM® Cortex®-M0+

64KB Flash, analog functions, timers and communication interfaces.

V1.0.8

Features

- **Ultra-low power operation environment**
  - Supply voltage range:1.8V to 5.5V
  - Temperature range:-40℃ to 85℃
  - Low power consumption mode: sleep mode, deep sleep mode
  - Operating power consumption: 70uA/MHz@64MHz
  - Power consumption in deep sleep mode: 75uA
  - Power consumption in deep sleep mode with partial power down: 6uA
  - Deep sleep with partial power down +32.768K + RTC: 7uA
- **Core**
  - ARM®32-bitCortex®-M0+ CPU
  - Operating frequency: 15KHz~64MHz
- **Memory**
  - 64KB Flash memory, shared program and data storage
  - 1KB dedicated data Flash memory
  - 4KB SRAM memory
- **Power and reset management**
  - Built-in power-on-reset (POR) circuit
  - Built-in voltage detection (LVD) circuit (threshold voltage can be set)
- **Clock management**
  - Built-in a high-speed oscillator with accuracy (±2%), and can provide 2MHz~64MHz system clock and peripheral module action clock
  - Built-in 15KHz low-speed oscillator
  - Supports 4MHz~16MHz external crystal oscillation
  - Supports 32.768KHz external crystal oscillator, which can be used to calibrate internal high-speed oscillators
- **High precision 12-bit ADC**
  - Conversion rate: 500Ksps
  - Number of external analog channels: 20
  - Supports single-channel conversion and multi-channel scanning conversion mode
  - Conversion range: 0 to positive reference voltage
- **GPIO**
  - Up to 22 GPIOs, supporting arbitrary allocation of digital functions
  - Most GPIOs support pull-up/down resistor function
  - All support key interrupt function
  - Built-in control circuit for clock output/buzzer output
- **Multiplier module**
  - Supports 32-bit multiplication operation
- **Linkage controller**
  - Able to link event signals together to achieve peripheral function linkage

    15 types of event input, 4 types of event trigger
- **Rich timer resources**
  - 16-bit timer: 8 channels, supports PWM output
  - 15-bit interval timer: 1
  - Real Time Clock (RTC): 1 (with perpetual calendar, alarm clock function, and supports a wide range of clock correction)
  - Watchdog timer (WDT): 1
  - SysTick Timer
- **Rich and flexible interfaces**
  - -2-channel serial communication unit, each channel can be freely configured as 1-channel standard UART or 2-channel SPI
  - Standard SPI: 1 channel (supports 8-bit and 16-bit)
  - Standard I^2C：1 channel
- **Supports 128-bit unique ID number (UID)**
  - Each chip has an individual ID number
- **Serial two-wire debugger (SWD)**
- **Package**
  - Support a variety of packages from 20-pin to 24-pin

1 Overview

1.1 Introduction

The Low-power CMS32L032 features a high-performance ARM® Cortex®-M0+ 32-bit RISC core operating at up to 64MHz with high-speed embedded Flash memory (up to 4KB for SRAM and 64KB for program/data Flash). This product integrates various standard interfaces such as I2C, SPI, UART, LIN, etc. Integrated a 12-bit A/D converter and temperature sensor(s). The 12bit A/D converter can be used to collect external sensor signals and reduce system design cost. The integrated temperature sensor(s) in the chip can realize real-time monitoring of the external environment temperature. Integrated 8-channel 16-bit timer module and EPWM control circuit, combined with the timers can realize the control of one DC motor or two stepper motors.

The CMS32L032 also has excellent low-power performance, supporting two low-power modes, sleep and deep sleep, for flexible design. Its operating power consumption is 70uA/MHz@64MHz and the power consumption in deep sleep mode with partial power down is only 7uA, making it suitable for low-power devices with battery power. Also, the integrated event-linked controller enables direct connection between hardware modules without CPU intervention, resulting in faster response than using interrupts, while reducing CPU activity frequency and extending battery life.

These features make the CMS32L032 microcontroller family suitable for a wide range of applications such as consumer electronics, motor drive control, home appliances and mobile devices.

1.2 Product model list

Product list of CMS32L032:

Number of pins	Package	Product model
20 pins	20-pin plastic TSSOP20 (6.5x4.4, 0.65mm pitch)	CMS32L032GE20SA
20 pins	20-pin plastic QFN (3x3mm, 0.4mm pitch)	CMS32L032GE20NB
24 pins	24-pin plastic SSOP24 (8.65x3.9, 0.635mm pitch)	CMS32L032GE24SS
24 pins	24-pin plastic QFN (4x4mm, 0.5mm pitch)	CMS32L032GE24NA

FLASH, SRAM capacity:

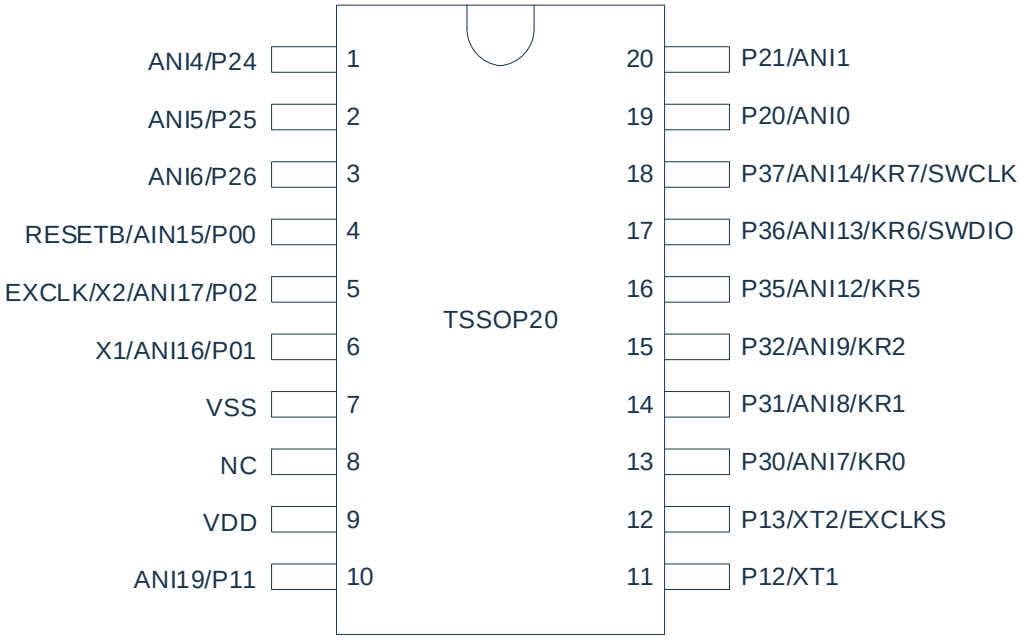
Flash Memory	Dedicated data Flash memory	SRAM	20 pins	24 pins
64KB	1KB	4KB	CMS32L032GE20	CMS32L032GE24

Product selection table for CMS32L032:

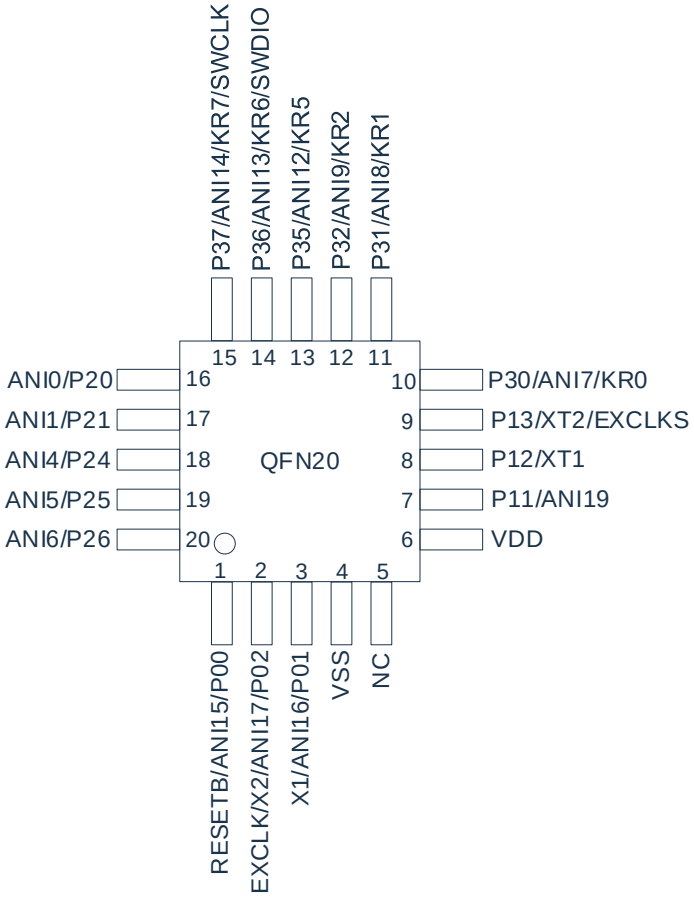
Part No.	Core	Main frequency (MHz)	Minimum operating voltage (V)	Maximum operating voltage (V)	Code Flash (KB)	SRAM (KB)	Data Flash (KB)	GPIO	12bit ADC	General-purpose timer (16bit)	Real Time Clock (RTC)	Watchdog Timer (WDT)	Asynchronous Serial Bus (UART)	Synchronous Serial Bus (SPI)	IIC Bus	LIN Bus	Hardware Multipliers	Package
CMS32L032 GE20SA	M0+	64	1.8	5.5	64	4	1	17	15	8	1	1	2	1	1	1	Y	TSSOP 20
CMS32L032 GE20NB	M0+	64	1.8	5.5	64	4	1	17	15	8	1	1	2	1	1	1	Y	QFN 20
CMS32L032 GE24SS	M0+	64	1.8	5.5	64	4	1	22	20	8	1	1	2	1	1	1	Y	SSOP 24
CMS32L032 GE24NA	M0+	64	1.8	5.5	64	4	1	22	20	8	1	1	2	1	1	1	Y	QFN 24

1.3 Top view

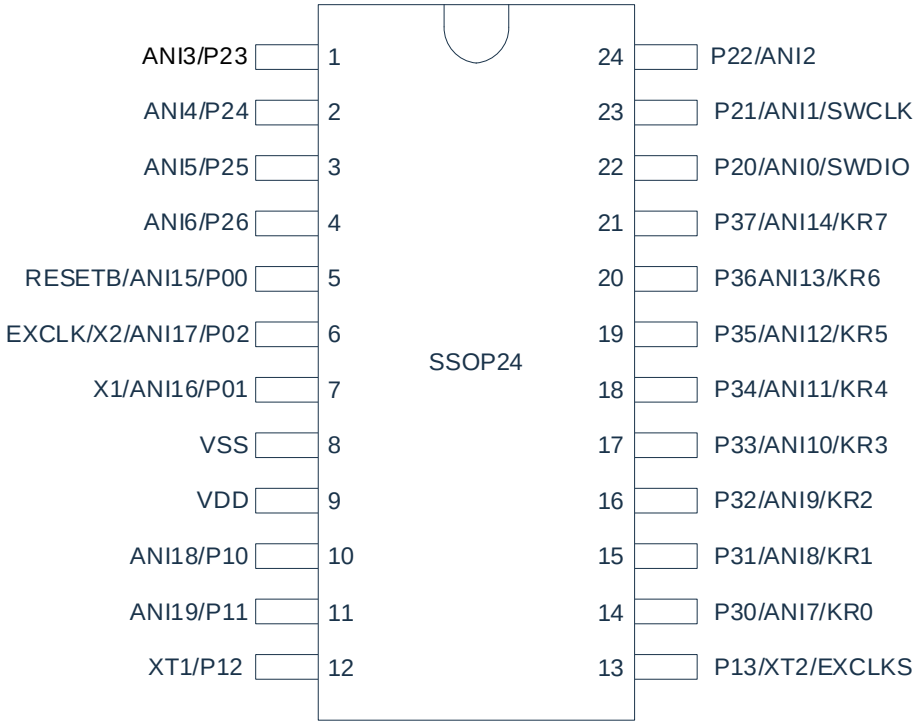
1.3.1 CMS32L032GE20SA



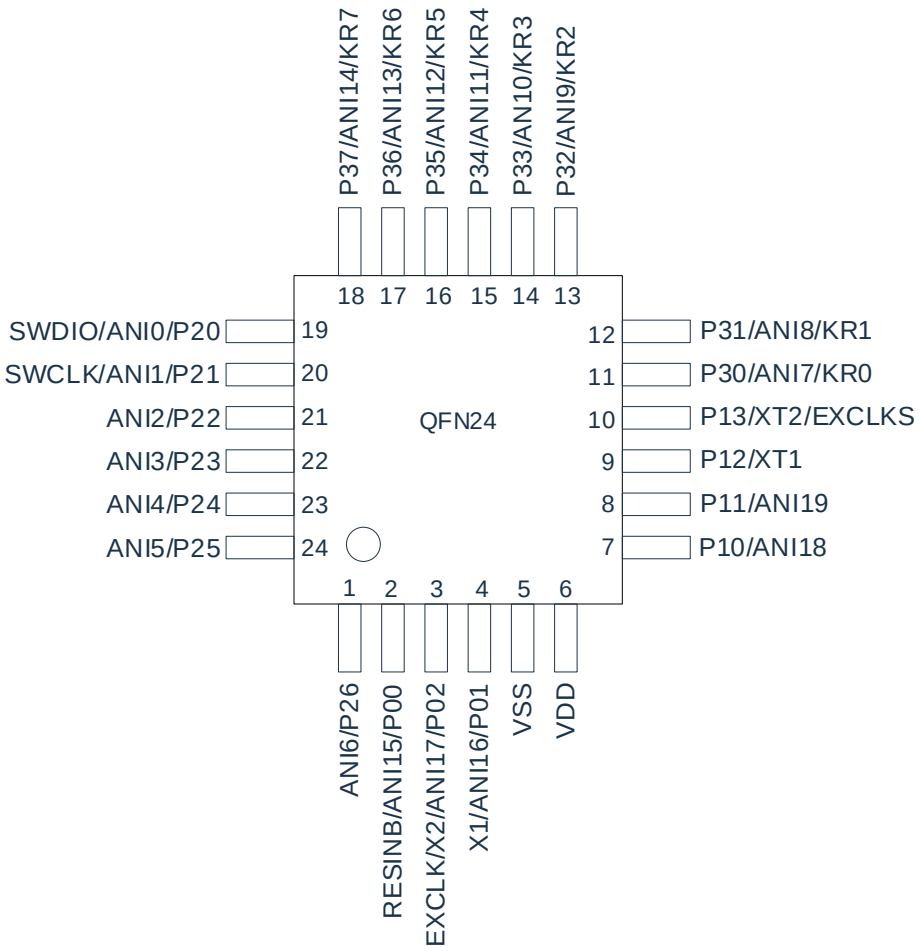
1.3.2 CMS32L032GE20NB



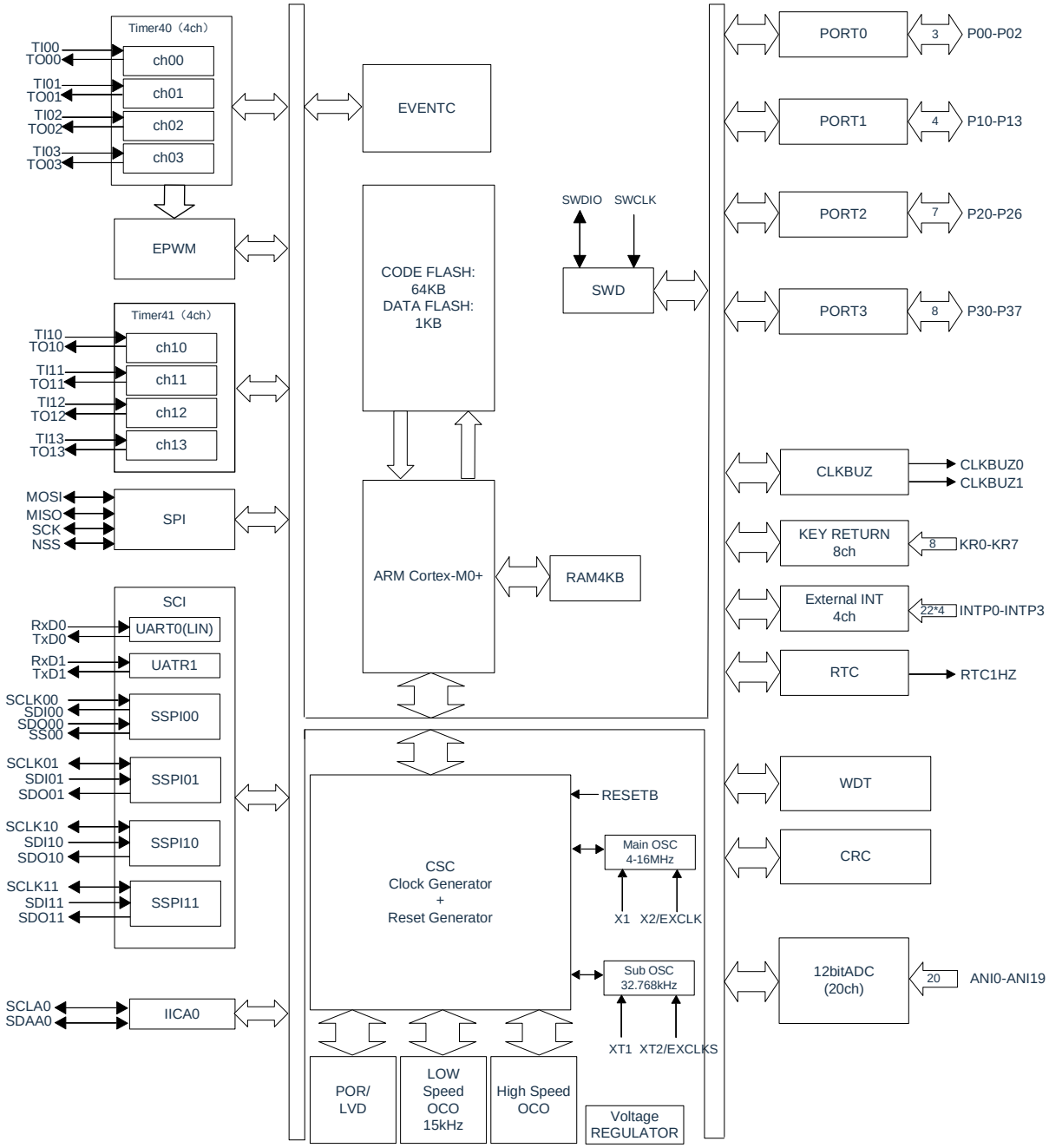
1.3.3 CMS32L032GE24SS



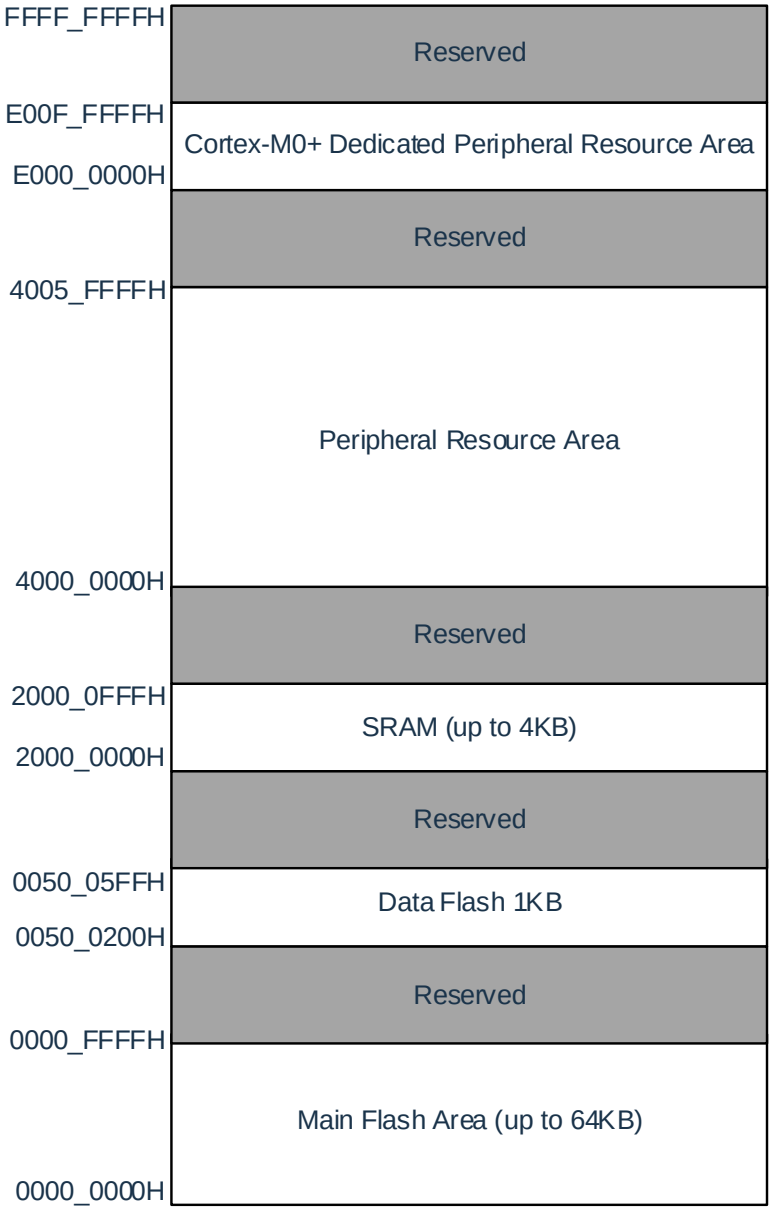
1.3.4 CMS32L032GE24NA



2 Product Block Diagram



3 Memory Mapping



4 Pin Function

4.1 Port function

Explanation of symbols in the table: I/O indicates digital input/output, I indicates digital input, O indicates digital output, AI indicates analog input, and AO indicates analog output.

Pin No.				Pin Name	Pin Type	Description
TSSOP20	QFN20	SSOP24	QFN24			
4	1	5	2	P00	I/O	GPIO configuration of input and output, pull-up through registers
				ANI15	AI	ADC channel 15 input
				RESINB	I	External reset
6	3	7	4	P01	I/O	GPIO configuration of input and output, pull-up and pull-down through registers
				ANI16	AI	ADC channel 16 input
				X1	AO	High-speed crystal output pin
5	2	6	3	P02	I/O	GPIO configuration of input and output, pull-up and pull-down through registers
				ANI17	AI	ADC channel 17 input
				X2	AI	High-speed crystal input pin
				EXCLK	I	External high-speed clock input pin
-	-	10	7	P10	I/O	GPIO configuration of input and output, pull-up and pull-down through registers
				ANI18	AI	ADC channel 18 input
10	7	11	8	P11	I/O	GPIO configuration of input and output, pull-up and pull-down through registers
				ANI19	AI	ADC channel 19 input
11	8	12	9	P12	I/O	GPIO configuration of input and output through registers
				XT1	AO	Low-speed crystal output pin
12	9	13	10	P13	I/O	GPIO configuration of input and output through registers
				XT2	AI	Low-speed crystal input pin
				EXCLKS	I	External low-speed clock input pin
19	16	22	19	P20	I/O	GPIO configuration of input and output, pull-up and pull-down through registers

Pin No.				Pin Name	Pin Type	Description
TSSOP20	QFN20	SSOP24	QFN24			
				ANI0	AI	ADC channel 0 input
				SWDIO	I/O	SWD data port
20	17	23	20	P21	I/O	GPIO configuration of input and output, pull-up and pull-down through registers
				ANI1	AI	ADC channel 1 input
				SWDCLK	I/O	SWD clock port
--	-	24	21	P22	I/O	GPIO configuration of input and output, pull-up and pull-down through registers
				ANI2	AI	ADC channel 2 input
-	-	1	22	P23	I/O	GPIO configuration of input and output, pull-up and pull-down through registers
				ANI3	AI	ADC channel 3 input
1	18	2	23	P24	I/O	GPIO configuration of input and output, pull-up and pull-down through registers
				ANI4	AI	ADC channel 4 input
2	19	3	24	P25	I/O	GPIO configuration of input and output, pull-up and pull-down through registers
				ANI5	AI	ADC channel 5 input
3	20	4	1	P26	I/O	GPIO configuration of input and output, pull-up and pull-down through registers
				ANI6	AI	ADC channel 6 input
13	10	14	11	P30	I/O	GPIO configuration of input and output, pull-up and pull-down through registers
				ANI7	AI	ADC channel 7 input
				KR0	I	Key interrupt input 0
14	11	15	12	P31	I/O	GPIO configuration of input and output, pull-up and pull-down through registers
				ANI8	AI	ADC channel 8 input
				KR1	I	Key interrupt input 1
15	12	16	13	P32	I/O	GPIO configuration of input and output, pull-up and pull-down through registers
				ANI9	AI	ADC channel 9 input

Pin No.				Pin Name	Pin Type	Description
TSSOP20	QFN20	SSOP24	QFN24			
				KR2	I	Key interrupt input 2
-	-	17	14	P33	I/O	GPIO configuration of input and output, pull-up and pull-down through registers
				ANI10	AI	ADC channel 10 input
				KR3	I	Key interrupt input 3
-	-	18	15	P34	I/O	GPIO configuration of input and output, pull-up and pull-down through registers
				ANI11	AI	ADC channel 11 input
				KR4	I	Key interrupt input 4
16	13	19	16	P35	I/O	GPIO configuration of input and output, pull-up and pull-down through registers
				ANI12	AI	ADC channel 12 input
				KR5	I	Key interrupt input 5
17	14	20	17	P36	I/O	GPIO configuration of input and output, pull-up and pull-down through registers
				ANI13	AI	ADC channel 13 input
				KR6	I	Key interrupt input 6
				SWDIO	I/O	SWD data port
18	15	21	18	P37	I/O	GPIO configuration of input and output, pull-up and pull-down through registers
				ANI14	AI	ADC channel 14 input
				KR7	I	Key interrupt input 7
				SWDCLK	I/O	SWD clock port
7	4	8	5	V_{SS}	P	Grounding pin
9	6	9	6	V_{DD}	P	Supply voltage input pin

The CMS32L032 series digital resources can be mapped to any GPIO, and the following table shows the digital function configuration list.

Function name	Input/Output	PxxCFG	Description
Analog function	Input/Output	6'h00	Analog Channel
GPIO	Input	6'h00	Digital input channel
	Output		Digital output channel
	Open drain		Open drain output channel
INTP0	Input	6'h02	External interrupt request input 0, can configure rising edge, falling edge and double edge
INTP1	Input	6'h03	External interrupt request input 1, can configure rising edge, falling edge and double edge
INTP2	Input	6'h04	External interrupt request input 2, can configure rising edge, falling edge and double edge
INTP3	Input	6'h05	External interrupt request input 3, can configure rising edge, falling edge and double edge
TI00	Input	6'h06	External count clock for 16-bit Timer4 /Capture trigger unit 0 input channel 0
TI01	Input	6'h07	External count clock for 16-bit Timer4/Capture trigger unit 0 input channel 1
TI02	Input	6'h08	External count clock for 16-bit Timer4/Capture trigger unit 0 input channel 2
TI03	Input	6'h09	External count clock for 16-bit Timer4/Capture trigger unit 0 input channel 3
TI10	Input	6'h0a	External count clock for 16-bit Timer4/Capture trigger unit 1 input channel 0
TI11	Input	6'h0b	External count clock for 16-bit Timer4/Capture trigger unit 1 input channel 1
TI12	Input	6'h0c	External count clock for 16-bit Timer4/Capture trigger unit 1 input channel 2
TI13	Input	6'h0d	External count clock for 16-bit Timer4/Capture trigger unit 1 input channel 3
TO00	Output	6'h0e	Timer unit 0 output channel 0 of 16-bit Timer4
TO01	Output	6'h0f	Timer unit 0 output channel 1 of 16-bit Timer4
TO02	Output	6'h10	Timer unit 0 output channel 2 of 16-bit Timer4
TO03	Output	6'h11	Timer unit 0 output channel 3 of 16-bit Timer4
TO10	Output	6'h12	Timer unit 1 output channel 0 of 16-bit Timer4
TO11	Output	6'h13	Timer unit 1 output channel 1 of 16-bit Timer4
TO12	Output	6'h14	Timer unit 1 output channel 2 of 16-bit Timer4
TO13	Output	6'h15	Timer unit 1 output channel 3 of 16-bit Timer4
SCLA0	Input/Output	6'h16	Clock input/output for serial interface IIC0
SCAA0	Input/Output	6'h17	Data input/output for serial interface IIC0
CLKBUZ0	Output	6'h18	Clock output/buzzer output 0
CLKBUZ1	Output	6'h19	Clock output/buzzer output 1

Function name	Input/Output	PxxCFG	Description
RTC1HZ	Output	6'h1a	Calibration clock output for real time clock
Reserved	-	6'h1b	Reserved
SPI_SSI	Input	6'h1c	SPI slave selection
SPI_MOSI	Output/Input	6'h1d	SPI master output slave input
SPI_MISO	Input/Output	6'h1e	SPI master input slave output
SPI_CLKOI	Output/Input	6'h1f	SPI clock
Reserved	-	6'h20	Reserved
Reserved	-	6'h21	Reserved
Reserved	-	6'h22	Reserved
Reserved	-	6'h23	Reserved
Reserved	-	6'h24	Reserved
Reserved	-	6'h25	Reserved
SAU0_SS	Input	6'h26	Serial communication unit SAU0 as SPI communication slave selection
SAU1_SS	Input	6'h27	Serial communication unit SAU1 as SPI communication slave selection
SCLKOI00	Output/Input	6'h28	Serial communication unit SAU0 unit 0 as SPI clock input/output
SCLKOI01	Output/Input	6'h29	Serial communication unit SAU0 unit 1 as SPI clock input/output
SCLKOI10	Output/Input	6'h2a	Serial communication unit SAU1 unit 0 as SPI clock input/output
SCLKOI11	Output/Input	6'h2b	Serial communication unit SAU1 unit 1 as SPI clock input/output
SDI00/RxD0	Input	6'h2c	Serial communication unit SAU0 unit 0 data input / serial port 0 input
SDI01	Input	6'h2d	Serial communication unit SAU0 unit 1 data input
SDI10/RxD1	Input	6'h2e	Serial communication unit SAU1 unit 0 data input / serial port 1 input
SDI11	Input	6'h2f	Serial communication unit SAU1 unit 1 data input
SDO00/TxD0	Output	6'h30	Serial communication unit SAU0 unit 0 data output / serial port 0 output
SDO01	Output	6'h31	Serial communication unit SAU0 unit 1 data output
SDO10/TxD1	Output	6'h32	Serial communication unit SAU1 unit 0 data output / serial port 1 output
SDO11	Output	6'h33	Serial communication unit SAU1 unit 1 data output
Reserved	-	6'h34	Reserved
Reserved	-	6'h35	Reserved
Reserved	-	6'h36	Reserved
Reserved	-	6'h37	Reserved
EPWMO00	Output	6'h38	EPWM channel 0 output
EPWMO01	Output	6'h39	EPWM channel 1 output
EPWMO02	Output	6'h3a	EPWM channel 2 output
EPWMO03	Output	6'h3b	EPWM channel 3 output
EPWMO04	Output	6'h3c	EPWM channel 4 output
EPWMO05	Output	6'h3d	EPWM channel 5 output
EPWMO06	Output	6'h3e	EPWM channel 6 output
EPWMO07	Output	6'h3f	EPWM channel 7 output

5 Function Summary

5.1 ARM® Cortex®-M0+ core

ARM's Cortex-M0(+) processor is a new generation of ARM processors for embedded systems. It provides a low-cost platform designed to meet the needs of low-pin-count and low-power microcontrollers while providing excellent computational performance and advanced system response to interrupts.

The Cortex-M0(+) processor is a 32-bit RISC processor that offers superior code efficiency, providing the high performance expected from an ARM core, differentiating it from 8- and 16-bit devices of equivalent memory size. The Cortex- M0(+) processor has 32 address lines and up to 4G of memory.

The CMS32L032 uses an embedded ARM core and is therefore compatible with all ARM tools and software.

5.2 Memory

5.2.1 Flash memory

The CMS32L032 has built-in flash memory that can be programmed, erased and rewritten. The following functions are available:

- Shared 64K storage space for programs and data.
- 1KB dedicated data Flash memory
- Support page erase, each page size is 512-byte, erase time 2ms
- Support byte/half-word programming, programming time 120us

5.2.2 SRAM

The CMS32L032 has a built-in 4K bytes of embedded SRAM.

5.3 Linkage controller

The linkage controller interlinks the events output by each peripheral function with the trigger source of the peripheral function. This enables direct collaborative operation between peripheral functions without using the CPU.

The linkage controller has the following functions:

- Able to link event signals together for linkage of peripheral function
- 5 types of event inputs and 4 types of event triggers.

5.4 Clock generation and start-up

A clock generation circuit is a circuit that generates a clock to the CPU and peripheral hardware. There are three types of system clocks and clock oscillation circuits.

5.4.1 Main system clock

- X1 oscillator circuit: It can generate 4~16MHz clock oscillation by connecting resonators to the pins (X1 and X2), and can stop oscillation by executing deep sleep command or setting MSTOP.
- High-speed internal oscillator (high-speed OCO): Oscillation can be performed by selecting the frequency by the option byte. After unreset, the CPU starts running at this high-speed internal oscillator clock by default. Oscillation can be stopped by executing a deep sleep command or setting the HIOSTOP bit. The frequency set by the option byte can be changed through the frequency selection register of the high-speed internal oscillator. The maximum frequency is 64MHz with an accuracy ± 2.0%.
- Input external clock from pin (X2): (4~16MHz), and the input of the external main system clock can be invalidated by executing the deep sleep command or setting the MSTOP bit.

5.4.2 Subsystem clock

- XT1 oscillator circuit: It can generate 32.768KHz clock oscillation by connecting a 32.768KHz resonator to the pins (XT1 and XT2), and can stop the oscillation by setting the XTSTOP bit.
- External clock input from pin (XT2): 32.768KHz and the ability to disable the external clock input by setting the XTSTOP bit.

5.4.3 Low-speed internal oscillator clock

ow-speed internal oscillator (low-speed OCO): It can generate 15KHz (TYP) clock oscillation. The low-speed internal oscillator clock can be used as the CPU clock. The following peripheral hardware can operate through the low-speed internal oscillator clock:

- Watchdog Timer (WWDT)
- Real Time Clock (RTC)
- 15-Bit Interval Timer

5.5 Power management

5.5.1 Power supply method

V_{DD}: External power supply, and voltage range is 1.8 to 5.5V.

5.5.2 Power-on-reset

The power-on-reset circuit (POR) has the following functions:

- An internal reset signal is generated when power is applied. If the supply voltage (V_{DD}) is greater than the detection voltage (V_{POR}), the reset is released. However, the reset state must be maintained by a voltage detection circuit or an external reset until the operating voltage range is reached.
- The power supply voltage (V_{DD}) is compared with the detection voltage (V_{POR}) and an internal reset signal is generated when $V_{DD} < V_{POR}$. However, when the power supply drops, it must be shifted to deep sleep mode or set to reset by voltage detection circuit or external reset before it is less than the operating voltage range. To restart operation, it must be confirmed that the power supply voltage has returned to the operating voltage range.

5.5.3 Voltage detection

The voltage detection circuit sets the operation mode and detection voltage (V_{LVDH}, V_{LVDL}, V_{LVD}) by means of option bytes. The voltage detection (LVD) circuit has the following functions:

- The internal reset or interrupt request signal is generated by comparing the power supply voltage (V_{DD}) with the detection voltage (V_{LVDH}, V_{LVDL}, V_{LVD}).
- The detection voltage of the supply voltage (V_{LVDH}, V_{LVDL}, V_{LVD}) can be selected via the option byte.
- Able to run in deep sleep mode.
- When the power supply rises, the reset state must be maintained by voltage detection circuitry or external reset before the operating voltage range is reached. When the power supply drops, it must be shifted to deep sleep mode or set to reset state by voltage detection circuit or external reset before it is less than the operating voltage range.
- The operating voltage range varies according to the setting of the user option byte.

5.6 Low-power consumption mode

The CMS32L032 supports two low-power modes to achieve the best compromise between low power consumption, short start-up time, and available wake-up sources:

- Sleep mode: Enter the sleep mode by executing a sleep instruction. Sleep mode is the mode that stops the CPU from running the clock. Before setting the sleep mode, if the high-speed system clock oscillation circuit, high-speed internal oscillator, or subsystem clock oscillator circuit is oscillating, then each clock continues to oscillate. Although this mode does not reduce the operating current to the point in deep sleep mode, it is an effective mode when you want to restart processing immediately with an interrupt request or when you want to intermittent run frequently.
- Deep sleep mode: Enter the deep sleep mode by executing a deep sleep instruction. Deep sleep mode is a mode that stops the oscillation of the high-speed system clock oscillator circuit and the high-speed internal oscillator and stops the whole system. It can significantly reduce the operating current of the chip. Intermittent operation is also possible because deep sleep mode can be released by interrupt requests. However, in the case of the X1 clock, the sleep mode must be selected if processing must start immediately by interrupt requests because a waiting time is required to ensure stable oscillation when the deep sleep mode is released.
- Deep sleep mode with partial power down: The deep sleep mode with partial power down is allowed by a pre-configured PMUKEY instruction and executed by a deep sleep instruction. Deep sleep mode with partial power-down is a mode that disables the peripheral power supply, and further reduces the chip's operating current compared to deep sleep mode. Partial power-down deep sleep mode can be released by external interrupts, key-in interrupts, RTC interrupts, 15-bit interval interrupts and WDT interrupt requests, so intermittent operation is also possible.

In any of the modes except the deep sleep mode with partial power down, the registers, flags and data memory all remain as they were before being set to standby mode, and the state of the output latches and output buffers of the input/output ports are also maintained. Partial power-down deep sleep mode requires reinitialization of peripheral module functions when it is released.

5.7 Reset function

The following 6 methods generate reset signals.

1) An external reset is input via the RESETB pin.
2) An internal reset is generated by program runaway detection by the watchdog timer.
3) An internal reset is generated by comparing the supply voltage and the detection voltage of the power-on-reset (POR) circuit.
4) An internal reset is generated by comparing the supply voltage and the detection voltage of the voltage detection circuit (LVD).
5) An internal reset occurred due to access to illegal memory.
6) Software reset.

The internal reset is the same as the external reset, and the program execution starts from writing at addresses 0000H and 0001H after the reset signal is generated.

5.8 Interrupt function

The Cortex-M0+ processor has a built-in nested vector interrupt controller (NVIC) that supports up to 32 interrupt request (IRQ) inputs and a non-maskable interrupt (NMI) input, in addition to multiple internal exceptions.

This product handles 32 maskable interrupt requests (IRQs) and a non-maskable interrupt (NMI), as detailed in the corresponding section of the user's manual. The actual number of interrupt sources varies from product to product.

5.9 Real time clock (RTC)

The Real Time Clock (RTC) has the following functions.

- Having counters of year, month, week, day, hour, minute, and second.
- Constant-period interrupt function (period: 0.5 seconds, 1 second, 1 minute, 1 hour, 1 day, 1 month)
- Alarm interrupt function (alarm: week, hour, minute)
- Pin output function of 1 Hz
- Supports sub-system clock or division of the master system clock as the operating clock for the RTC.
- The real-time clock interrupt signal (INTRTC) can be used as a deep sleep mode wake-up.
- Supports a wide range of clock correction functions.

Year, month, week, day, hour, minute, and second counts can only be performed if the subsystem clock (32.768KHz) or the division of the main system clock is selected as the operating clock of the RTC. When a low-speed internal oscillator clock (15KHz) is selected, only the constant-period interrupt function can be used.

5.10 Watchdog timer

The 1-channel WWDT, 17-bit watchdog timer runs with option byte set count. The watchdog timer runs with a low internal oscillator clock (15KHz). The watchdog timer is used to detect a program runaway. An internal reset signal is generated when a program runaway is detected.

The following situations are judged to be out of control:

- When watchdog timer counter overflow occurs
- When writing data other than "ACH" to the WDTE register
- When writing data to the WDTE register during window closure

5.11 SysTick timer

This timer is specific to real-time operating systems, but can also be used as a standard decrement counter.

It features a 24-bit decrement counter when the self-loading capacity counter reaches 0, and a maskable system interrupt is generated.

5.12 Timer4

The product has two Timer4 units with four channels of 16-bit timers, each of which can be used separately as an independent timer or combined with multiple channels for advanced timer functions.

For details of each function, please refer to the following table.

Independent channel operation function	Multi-channel linkage operation function
● Interval timer ● Square wave output ● External event counter ● Frequency divider ● Measurement of input pulse interval ● Measurement of the high/low level width of the input signal ● Delay counter	● Single trigger pulse output ● PWM output ● Multiple PWM outputs

5.12.1 Independent channel operation function

The independent channel operation function is a function to use any channel independently of other channel operating modes. The independent channel operation feature is used as the following mode:

1) Interval timer: Can be used as a reference timer to generate interrupts (INTTM) at fixed intervals.
2) Square wave output: Whenever an INTTM interrupt is generated, it triggers a flip and outputs a 50% duty cycle square wave from the timer output pin (TO).
3) External event counter: Counts the valid edges of the input signal of the timer input pin (TI) and can be used as an event counter for generating interrupts if the specified number of times is reached.
4) Divider function (channel 0 of unit 0 only): Divides the input clock of the timer input pin (TI00) and outputs it from the output pin (TO00).
5) Measurement of input pulse interval: The input pulse interval is measured by starting counting at the active edge of the input pulse signal at the timer input pin (TI) and capturing the count value at the active edge of the next pulse.
6) Measurement of the high/low width of the input signal: The width of the high or low level of the input signal is measured by starting counting on one edge of the input signal at the timer input pin (TI) and capturing the count value on the other edge.
7) Delay counter: starts counting at the valid edge of the input signal of the timer input pin (TI) and generates an interrupt after an arbitrary delay period.

5.12.2 Multi-channel linkage operation function

The multi-channel linkage function is a function that combines a master channel (the reference timer for the main control cycle) and a slave channel (the timer that operates in compliance with the master channel). The multi-channel linkage function can be used in the following modes:

1) Single trigger pulse output: Use 2 channels in pairs to generate a single trigger pulse with arbitrary output timing and pulse width
2) PWM (Pulse Width Modulation) output: Use two channels in pairs to generate pulses with an arbitrary set period and duty cycle.
3) Multiple PWM (Pulse Width Modulation) Outputs: Can generate up to seven PWM signals with any duty cycle by extending the PWM function and using one master channel and multiple slave channels with a fixed period.

5.12.3 8-bit timer operation function

The 8-bit timer operation function allows the 16-bit timer channel to be used as the function of two 8-bit timer channels. (Only channel 1 and channel 3 can be used).

5.12.4 LIN-bus support function

Timer4 unit can be used to check whether the received signal in LIN-bus communication is suitable for LIN-bus communication format.

1) Wake-up signal detection: The low-level width is measured by starting counting on the falling edge of the input signal on the UART serial data input pin (RxD) and capturing the count value on the rising edge. If the low width is greater than or equal to a fixed value, it is considered a wake-up signal.
2) Detection of the break field: After a wake-up signal is detected, the low-level width is measured by starting counting from the falling edge of the input signal of the UART serial data input pin (RxD) and capturing the count value on the rising edge. If the width of the low-level is greater than or equal to a fixed value, it is considered to be a break field.
3) Measurement of sync field pulse width: After detecting the break field, measure the low- and high-level widths of the input signal of the UART serial data input pin (RxD). Based on the bit space of the sync field measured in this way, the baud rate is calculated.

5.13 EPWM output control circuit

This is achieved using the PWM output function of Timer4. This EPWM with deadband control output enables the control of a DC motor or two stepper motors.

5.14 15-bit interval timer

This product has a built-in 15-bit interval timer that generates interrupts (INTIT) at any pre-set interval and can be used to wake up from deep sleep mode.

5.15 Clock output/buzzer output control circuit

The clock output controller is used to provide a clock to the peripheral IC and the buzzer output controller is used to output a square wave of buzzer frequency. The clock output or buzzer output is implemented by a dedicated pin.

5.16 General-purpose serial communication unit

This product has 2 built-in universal serial communication units with up to 2 serial communication channels per unit. It can realize the communication function of standard SPI, simplified SPI and UART .

5.16.1 3-wire serial interface (simplified SPI)

Synchronizes with the serial clock (SCK) output from the master device for data transmission and reception.

This is a clock-synchronous communication interface that uses a serial clock (SCK), a transmit serial data (SO), and a receive serial data (SI) for communication on a total of three communication lines.

[Data transmitting and receiving]

- Data length of 7~16 bits
- Phase control of transmitted and received data
- MSB/LSB preferred option

[Clock control]

- Choice of master or slave
- Phase control of input/output clocks
- Transmission period generated by prescalers and channel internal counters
- Maximum transmission rate

  Master communication: Max $F_{CLK}/2$

  Slave communication: Max $F_{MCK}/6$

[Interrupt function]

- End-of-transfer interrupt, buffer null interrupt

[Error detection flag]

- Overflow error

5.16.2 Simplified SPI with slave chip selection

SPI serial communication interface supports slave chip select input function. This is a clock-synchronous communication interface that uses a slave chip select input (SSI), a serial clock (SCK), a transmit serial data (SO), and a receive serial data (SI) to communicate with a total of four communication lines.

[Data transmitting and receiving]

- Data length of 7-bit~16-bit
- Phase control of transmitted and received data
- MSB/LSB preferred option
- Level setting for transmitd and received data

[Clock control]

- Phase control of input/output clocks
- Transmission period generated by prescaler and channel internal counter
- Maximum transmission rate

  Slave communication: Max F_{MCK}/6

[Interrupt function]

- End-of-transfer interrupt, buffer null interrupt

[Error detection flag]

- Overflow error

5.16.3 UART

The function of asynchronous communication via a total of 2 lines, serial data transmission (TxD) and serial data reception (RxD). Using these two communication lines, data is transmitted and received asynchronously (using the internal baud rate) with other communicating parties by data frame (consisting of start bits, data, parity bits, and stop bits). Full-duplex UART communication can be achieved by using a total of 2 channels dedicated to transmit (even channel) and receive (odd channel), and LIN-bus can be supported by combining timer4 units and external interrupts (INTP0).

[Data transmitting and receiving]

- Data length of 7, 8, 9 or 16 bits
- MSB/LSB preferred option
- Level setting and inverted phase selection of transmitted and received data
- Appending for parity bits, parity-check function
- Appending for stop bits, detection of stop bits

[Interrupt function]

- End-of-transfer interrupt, buffer null interrupt
- False interrupts caused by frame errors, parity errors, or overflow errors

[Error detection flag]

- Frame error, parity error, overflow error

[LIN-bus function]

- Detection of wake-up signals
- Detection of break field (BF)
- Measurement of sync field, calculation of baud rate

5.17 Standard serial interface SPI

The serial interface SPI has the following 2 modes:

- Run-stop mode: This is the mode used when serial transmission is not performed, which can reduce power consumption.
- 3-wire serial I/O mode: This mode allows 8-bit or 16-bit data transfer with multiple devices via 3 lines of the serial clock (SCK) and serial data buses (MISO and MOSI).

5.18 Standard serial interface IICA

The serial interface IICA has the following 3 modes:

- Run-stop mode: This is the mode used when serial transmission is not performed, which can reduce power consumption.
- I^2C-bus mode (supports multiple masters): This mode allows 8-bit data transfer with multiple devices via two lines of the serial clock (SCLA) and serial data bus (SDAA). Compliant with the I^2C bus format, the master device can generate "start condition", "address", "indication of transfer direction", "data" and "stop condition" to the slave devices on the serial data bus. The slave device automatically detects the received status and data by hardware. This function simplifies the I^2C bus control part of the application. Because the SCLA and SDAA pins of the serial interface IICA are used as open-drain outputs, pull-up resistors are required for the serial clock line and the serial data bus.
- Wakeup mode: In deep sleep mode, it can release deep sleep mode by generating an interrupt request signal (INTIICA) when an extension code or local station address is received from the master device. It is set by IICA control register.

5.19 Analog-to-Digital Converter (ADC)

This product has a built-in 12-bit resolution analog-to-digital converter, SARADC, which converts analog inputs to digital values and supports up to 20 channels of ADC analog inputs (ANI0~ANI19). The ADC contains the following functions:

- 12-bit resolution, slew rate: 500Ksps.
- Triggering mode: supports software triggering, hardware triggering and hardware triggering in standby state
- Channel selection: supports both single channel selection and multi-channel scanning
- Conversion mode: supports single conversion and continuous conversion
- Operating voltage: supports 1.8V ≤ VDD ≤ 5.5V operating voltage range
- Built-in reference voltage (1.45V) and temperature sensors can be detected.

The ADC can set various A/D conversion modes with the following mode combinations.

Trigger mode	Software trigger	Start conversions by operating the software
	Hardware trigger no-wait mode	Start conversions by detecting a hardware trigger.
	Hardware trigger wait mode	In the conversion standby state where the power is cut off, the power is turned on by detecting the hardware trigger, and the conversion starts automatically after the A/D power stabilization waiting time.
Channel selection mode	Select mode	Select 1 channel of analog input for A/D conversion.
	Scan mode	Perform A/D conversion of 4 channels of analog input in sequence. 4 consecutive channels from ANI0 to ANI15 can be selected as analog inputs.
Conversion mode	Single conversion mode	Perform 1 A/D conversion for the selected channel.
	Continuous conversion mode	Continuous A/D conversion of the selected channel until it is stopped by the software.
Sampling time/ conversion time	Number of sampling clocks/conversion clocks	The sampling time can be set by the register, and the number of sampling clocks can be set to 4 clk (default) or 8 clk. When the number of sampling clocks is 4 clk, the total number of sampling + conversion clocks is 16 clk.

5.20 Two-wire serial debug port (SW-DP)

SW-DP interface of ARM allows connection to the microcontroller via serial line debug tools.

5.21 Security function

5.21.1 Flash CRC operation function (high-speed CRC, general-purpose CRC)

Data errors in flash memory are detected by CRC operations.

The following 2 CRCs can be used separately according to different applications and usage conditions.

- High-speed CRC: In the initialization program, it can stop CPU operation and check the whole code flash area at high speed.
- General-purpose CRC: In CPU operation, it is not limited to the code flash memory area but can be used for multi-purpose inspection.

5.21.2 SFR protection function

It prevents rewriting of important SFR (Special Function Register) due to CPU runaways.

5.21.3 Illegal memory access detection function

It detects illegal access to illegal memory areas (areas without memory or areas with restricted access).

5.21.4 Frequency detection function

It can self detect the CPU or peripheral hardware clock frequency by Timer4 unit.

5.21.5 A/D testing function

The A/D converter is self-tested by performing A/D conversion of the positive (+) reference voltage, negative (-) reference voltage, analog input channel (ANI), temperature sensor output voltage, and internal reference voltage of the A/D converter.

5.21.6 Digital output signal level detection function of input/output ports

The output level of the pin can be read when the input/output ports are in output mode.

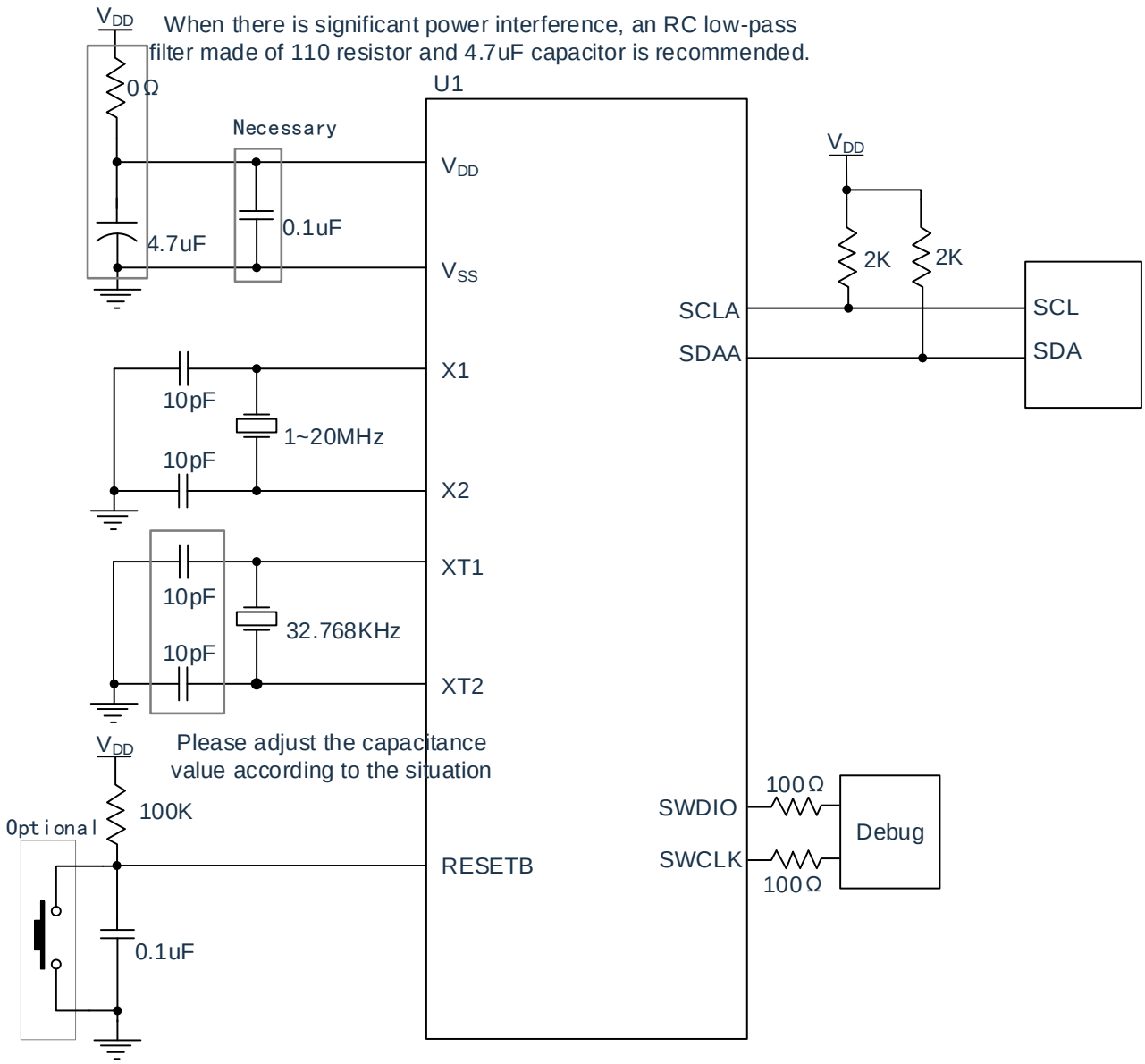
5.22 Key function

A key interrupt (INTKR) can be generated by inputting a falling edge on the key interrupt input pins (KR0 ~ KR7).

6 Electrical Characteristics

6.1 Typical application peripheral circuits

The device connections of peripheral circuits for typical MCU applications are referenced as follows:



6.2 Absolute maximum voltage ratings

(T_A= -40~85℃)

Item	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD}		-0.5~6.5	V
Input voltage	V_I	P00~P02, P10~P13, P20~P26, P30~P37 EXCLK, EXCLKS	-0.3~V_{DD}+0.3 Note1	V
Output voltage	V_O	P00~P02, P10~P13, P20~P26, P30~P37	-0.3~V_{DD}+0.3 Note 1	V
Analog input voltage	V_{AI}	ANI0~ANI19	-0.3~V_{DD}+0.3	V

Note 1: No more than 6.5V.

Notice: Even if one item of the list instantly exceeds the absolute maximum rating, the quality of the product may be reduced. The absolute maximum rating is the rating that may bring physical damage to the product, and the product must be used in a state where the rating is not exceeded.

Remark:

1. Unless otherwise specified, the characteristics of multiplexed pins are the same as those of port pins.
2. Use V_{SS} as the reference voltage.
3. Low temperature specification values are guaranteed by design, and low temperature conditions are not tested in mass production.

6.3 Absolute maximum current ratings

(T_A= -40~85˚C)

Item	Symbol	Condition		Min	Typ
High level output current	I_{OH1}	Per pin	P00~P02, P10~P11, P20~P26, P30~P37	-10	mA
		Total pins	P10~P11, P30~P35	-50	mA
			P00~P02, P20~P26, P36~P37	-70	mA
	I_{OH2}	Per pin	P12~P13	-3	mA
		Total pins		-6	mA
Low level output current	I_{OL1}	Per pin	P00~P02, P10~P13, P20~P26, P30~P37	20	mA
		Total pins	P10~P11, P30~P35	60	mA
			P00~P02, P20~P26, P36~P37	70	mA
	I_{OL2}	Per pin	P12~P13	10	mA
		Total pins		20	mA
Working environment temperature	T_A	Usual runtime		-40~85	˚C
		When flash memory is programmed			
Storage temperature	T_{stg}	-		-65~150	˚C

Notice: Even if one item of the list instantly exceeds the absolute maximum rating, the quality of the product may be reduced. The absolute maximum rating is the rating that may bring physical damage to the product, and the product must be used in a state where the rating is not exceeded.

Remark:

1. Unless otherwise specified, the characteristics of multiplexed pins are the same as those of port pins.
2. Low temperature specification values are guaranteed by design, and low temperature conditions are not tested in mass production.

6.4 Oscillation circuit characteristics

6.4.1 X1, XT1 characteristics

(T_A= -40~85℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition	Min	Typ	Max	Unit
X1 clock oscillation frequency (F_X)	Ceramic Resonators / Crystal Resonators	1.8V≤V_{DD}≤5.5V	4.0	-	16.0	MHz
XT1 clock oscillation frequency (F_{XT})	Crystal Resonators	1.8V≤V_{DD}≤5.5V	32	32.768	35	KHz

Remark:

1. It only indicates the frequency tolerance range of the oscillation circuit. Please refer to AC Characteristics for the instruction execution time.
2. Please entrust the resonator manufacturer with an evaluation after installing the circuit and use it after checking the oscillation characteristics.
3. Low temperature specification values are guaranteed by design, and low temperature conditions are not measured in mass production.

6.4.2 Internal oscillator characteristics

(T_A= -40~85℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Resonator	Condition	Min	Typ	Max	Unit
Clock frequency of high-speed internal oscillator (F_{IH})Note 1,2	-	1.0	-	64.0	MHz
High-speed internal oscillator clock frequency accuracy	TA= -20~70℃	-2	-	+2	%
	TA= -40~85℃	-2.5	-	+2.5	%
Clock frequency of the low-speed internal oscillator (F_{IL})	-	13.5	15	16.5	KHz

Note 1: The frequency of the high-speed internal oscillator is selected via the option byte.

Note 2: Only the characteristics of the oscillation circuit are indicated. Please refer to the AC characteristics for the instruction execution time.

Remark: Low temperature specification values are guaranteed by design, and low temperature conditions are not measured in mass production.

6.5 DC characteristics

6.5.1 Pin characteristics

(T_A= -40~85℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition		Min	Typ	Max	Unit
High level output current Note1	I_{OH1}	Per pin for P00~P02, P10~P11, P20~P26, P30~P37	1.8V≤V_{DD}≤5.5V -40~85℃	-	-	-8.0 Note 2	mA
		Total of P10~P11, P30~P35 (When duty≤70% Note 3)	4.0V≤V_{DD}≤5.5V -40~85℃	-	-	-40.0	mA
			2.4V≤V_{DD}<4.0V	-	-	-8.0	mA
			1.8V≤V_{DD}<2.4V	-	-	-4.0	mA
		Total of P00~P02, P20~P26, P36~P37 (When duty≤70% Note 3)	4.0V≤V_{DD}≤5.5V -40~85℃	-	-	-60.0	mA
			2.4V≤V_{DD}<4.0V	-	-	-10.0	mA
			1.8V≤V_{DD}<2.4V	-	-	-5.0	mA
		Total of all pins (When duty≤70% Note 3)	1.8V≤V_{DD}≤5.5V -40~85℃			-100	mA
	I_{OH2}	Per pin for P12~P13	1.8V≤V_{DD}≤5.5V	-	-	-2.0 Note 2	mA
		Total of all pins (When duty≤70% Note 3)	1.8V≤V_{DD}≤5.5V	-	-	-4	mA

Note 1: This is the current value that guarantees device operation even if current flows from the V_{DD} pin to the output pin(s).

Note 2: The total current value cannot be exceeded.

Note 3: This is the output current value for the condition "duty cycle ≤ 70% ". The output current value for a duty cycle > 70% can be calculated using the following equation (in the case of changing the duty cycle to n%).

Total output current of pins=(I_{OH}×0.7)/(n×0.01)

<Example>I_{OH}= -10.0mA, n=80%

Total output current of pins= (-10.0×0.7)/(80×0.01) ≈ -8.7mA

The current at each pin does not vary by duty cycle and does not flow above the absolute maximum rating.

Remark:

1. Unless otherwise specified, the characteristics of multiplexed pins are the same as those of port pins.
2. Low temperature specification values are guaranteed by design, and low temperature conditions are not measured in mass production.

(T_A= -40~85℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition		Min	Typ	Max	Unit
Low level output current Note1	I_{OL1}	Per pin for P00~P02, P10~P11 P20~P26, P30~P37	1.8V≤V_{DD}≤5.5V -40~85℃	-	-	18 Note 2	mA
		Total of P10~P11, P30~P35 (When duty≤70% Note 3)	4.0V≤V_{DD}≤5.5V -40~85℃	-	-	50	mA
			2.4V≤V_{DD}<4.0V	-	-	15	mA
			1.8V≤V_{DD}<2.4V	-	-	8	mA
		Total of P00~P02, P20~P26 P36~P37 (When duty≤70% Note 3)	4.0V≤V_{DD}≤5.5V -40~85℃	-	-	60	mA
			2.4V≤V_{DD}<4.0V	-	-	20	mA
			1.8V≤V_{DD}<2.4V	-	-	10	mA
		Total of all pins (When duty≤70% Note 3)	1.8V≤V_{DD}≤5.5V -40~85℃	-	-	80	mA
	I_{OL2}	Per pin for P12~P13	1.8V≤V_{DD}≤5.5V	-	-	10 Note 2	mA
		Total of all pins (When duty≤70% Note 3)	1.8V≤V_{DD}≤5.5V	-	-	16	mA

Note 1: This is the current value guarantees device operation if current flows from the output pin(s) to the V_{SS} pin.

Note 2: The total current value cannot be exceeded.

Note 3: This is the output current value for the condition "duty cycle ≤ 70% ". The output current value for a duty cycle > 70% can be calculated using the following equation (in the case of changing the duty cycle to n%).

Total output current of pins =(I_{OL}×0.7)/(n×0.01)

<Example>I_{OL}=10.0mA, n=80%

Total output current of pins =(10.0×0.7)/(80×0.01) ≈ 8.7mA

The current at each pin does not vary by duty cycle and does not flow above the absolute maximum rating.

Remark:

1. Unless otherwise specified, the characteristics of multiplexed pins are the same as those of port pins.
2. Low temperature specification values are guaranteed by design, and low temperature conditions are not measured in mass production.

(T_A= -40~85℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition	Min	Typ	Max	Unit
High level input voltage	V_{IH1}	P00~P02, P10~P13 P20~P26, P30~P37	0.7V_{DD}	-	V_{DD}	V
Low level input voltage	V_{IL1}	P00~P02, P10~P13 P20~P26, P30~P37	0	-	0.3V_{DD}	V

Remark:

1. Unless otherwise specified, the characteristics of multiplexed pins are the same as those of port pins.
2. Low temperature specification values are guaranteed by design, and low temperature conditions are not measured in mass production.

(T_A= -40~85℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition		Min	Typ	Max	Unit
High level output voltage	V_{OH1}	P00~P02, P10~P11 P20~P26, P30~P37	4.0V≤V_{DD}≤5.5V, I_{OH1}= -8.0mA	V_{DD}-1.5	-	-	V
			4.0V≤V_{DD}≤5.5V, I_{OH1}= -4.0mA	V_{DD}-0.7	-	-	V
			2.4V≤V_{DD}≤5.5V, I_{OH1}= -2.0mA	V_{DD}-0.6	-	-	V
			1.8V≤V_{DD}≤5.5V, I_{OH1}= -1mA	V_{DD}-0.5	-	-	V
	V_{OH2}	P12~P13	4.0V≤V_{DD}≤5.5V, I_{OH2}= -2mA	V_{DD}-1.5	-	-	V
			4.0V≤V_{DD}≤5.5V I_{OH2}= -1mA	V_{DD}-0.7	-	-	V
			2.4V≤V_{DD}≤5.5V I_{OH2}= -0.4mA	V_{DD}-0.6	-	-	V
			1.8V≤V_{DD}≤5.5V I_{OH2}= -0.2mA	V_{DD}-0.5	-	-	V
Low level output voltage	V_{OL1}	P00~P02, P10~P11 P20~P26, P30~P37	4.0V≤V_{DD}≤5.5V I_{OL1}=18.0mA	-	-	1.2	V
			4.0V≤V_{DD}≤5.5V I_{OL1}=9.0mA	-	-	0.6	V
			2.4V≤V_{DD}≤5.5V I_{OL1}=5.0mA	-	-	0.5	V
			1.8V≤V_{DD}≤5.5V I_{OL1}=2.0mA	-	-	0.4	V
	V_{OL2}	P12~P13	4.0V≤V_{DD}≤5.5V I_{OL2}=8.0mA	-	-	1.2	V
			4.0V≤V_{DD}≤5.5V I_{OL2}=4.0mA	-	-	0.7	V
			2.4V≤V_{DD}≤5.5V I_{OL2}=2mA	-	-	0.4	V
			1.8V≤V_{DD}≤5.5V I_{OL2}=1mA	-	-	0.4	V

Remark:

1. Unless otherwise specified, the characteristics of multiplexed pins are the same as those of port pins.
2. Low temperature specification values are guaranteed by design, and low temperature conditions are not measured in mass production.

(T_A= -40~85℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition		Min	Typ	Max	Unit
High level input leakage current	I_{LIH1}	P00, P10~P11 P20~P26, P30~P37	V_I=V_{DD}	-	-	1	μA
	I_{LIH2}	P01~P02, P12~P13	V_I=V_{DD}, in input port or external clock input	-	-	1	μA
			V_I=V_{DD}, when a resonator is connected	-	-	10	μA
Low level input leakage current	I_{LIL1}	P00, P10~P11 P20~P26, P30~P37	V_I=V_{SS}	-	-	-1	μA
	I_{LIL2}	P01~P02, P12~P13	V_I=V_{SS}, in input port or external clock input	-	-	-1	μA
			V_I=V_{SS}, when a resonator is connected	-	-	-10	μA
Internal pull-up resistance	R_U	P00~P02 P10~P11 P20~P26, P30~P37	V_I=V_{SS}, in input port	10	30	50	KΩ
Internal pull-down resistance	R_D	P00~P02 P10~P11 P20~P26, P30~P37	V_I=V_{DD}, in input port	10	30	50	KΩ

Remark:

1. Unless otherwise specified, the characteristics of multiplexed pins are the same as those of port pins.
2. Low temperature specification values are guaranteed by design, and low temperature conditions are not measured in mass production.

6.5.2 Supply current characteristics

(T_A= -40~85℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition				Min	Typ	Max	Unit
Supply current Note 1	I_{DD1}	Operating mode	High-speed internal oscillator	F_{HOCO}=64MHz, F_{IH}=64MHz Note 3		-	3.9	4.7	mA
				F_{HOCO}=64MHz, F_{IH}=32MHz Note 3		-	3.1	3.6	
			High-speed master system clock	F_{MX}=16MHz Note 2	Input the square wave	-	4.0	4.4	mA
					Connect the crystal oscillator	-	4.0	4.4	
			Subsystem clock operation	F_{SUB}=32.768KHz Note4	Input the square wave	-	150	300	uA
					Connect the crystal oscillator	-	150	300	
			Low-speed internal oscillator	F_{IL}=15KHz Note 8		-	150	300	uA
	I_{DD2}	Sleep mode	High-speed internal oscillator	F_{HOCO}=64MHz, F_{IH}=64MHz Note 3		-	1.4	2.2	mA
				F_{HOCO}=32MHz, F_{IH}=32MHz Note 3		-	1.1	1.6	
			High-speed master system clock	F_{MX}=16MHz Note 2	Input the square wave	-	0.8	1.2	mA
					Connect the crystal oscillator	-	0.8	1.2	
			Subsystem clock operation	F_{SUB}=32.768KHz Note5	Input the square wave	-	80	220	uA
					Connect the crystal oscillator	-	80	220	
			Low-speed internal oscillator	F_{IL}=15KHz Note 8		-	80	220	uA
	I_{DD3} Note 6	Deep sleep mode Note 7	-			-	75	180	uA
		Partial power-down deep sleep mode Note 7	T_A = -40~25℃ V_{DD}=3.0V			-	6.0	13	uA
			T_A = -40~85℃ V_{DD}=3.0V			-	6.0	80	uA

Note 1: This is the current flowing through V_{DD} and includes the input leakage current with the input pin fixed to V_{DD} or V_{SS} state. Typical value: CPU is in multiplication instruction execution (I_{DD1}), and does not include peripheral operating current. Maximum value: CPU in multiplication instruction execution (I_{DD1}) and includes peripheral operating current, but does not include the current flowing to the A/D converter, LVD circuit, I/O ports, internal

pull-up or pull-down resistors, or the current when rewriting the data flash.

Note 2: This is the case when the high-speed internal oscillator and the subsystem clock stop oscillating.

Note 3: This is the case when the high-speed main and subsystem clocks stop oscillating.

Note 4: This is the case when the high-speed internal oscillator and the high-speed master system clock stop oscillating.

Note 5: This is the case when the high-speed internal oscillator and high-speed master system clock stop oscillating. The current flow to the RTC is included, but the current flow to the 15-bit interval timer and watchdog timer is not included.

Note 6: The current flow to RTC, 15-bit interval timer and watchdog timer is not included. MDSET [1:0] of LCDM0 register needs to be set to b'11.

Note 7: For the current value when the subsystem clock is running in deep sleep mode, please refer to the current value when the subsystem clock is running in sleep mode.

Note 8: This is the case of a high-speed internal oscillator, where the high-speed master and subsystem clocks stop oscillating.

Remark:

1. F_{HOCO}: Clock frequency of the high-speed internal oscillator, F_{IH}: system clock frequency provided by the high-speed internal oscillator.
2. F_{SUB}: External subsystem clock frequency (XT1/XT2 clock oscillation frequency).
3. F_{MX}: External main system clock frequency (X1/X2 clock oscillation frequency).
4. F_{IL}: Clock frequency of the low-speed internal oscillator.
5. The temperature for typical values is T_A = 25°C.
6. Low temperature specification values are guaranteed by design, and low temperature conditions are not measured in mass production.

(T_A= -40~85°C, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition	Min	Typ	Max	Unit
Low-speed internal oscillator operating current	I_{FIL} Note 1	-	-	0.2	-	uA
RTC operating current	I_{RTC} Note 1,2,3	-	-	0.04	-	uA
15-bit interval timer operating current	I_{IT} Note 1,2,4	-	-	0.02	-	uA
Watchdog timer operating current	I_{WDT} Note 1,2,5	F_{IL}=15KHz	-	0.22	-	uA
A/D converter operating current	I_{ADC} Note 1,6	ADC @8MHz	-	1.0	-	mA
LVD operating current	I_{LVD} Note 1,7	-	-	0.08	-	uA

Note 1: This is the current flowing through V_{DD}.

Note 2: This is the case when the high-speed internal oscillator and the high-speed system clock stop oscillating.

Note 3: This is the current flowing to the real time clock (RTC) only (excluding the operating current of the low speed internal oscillator and XT1 oscillator circuit). In the case of real-time clock operation in run mode or sleep mode, the microcontroller current value is the value of I_{DD1} or I_{DD2} plus I_{RTC}. In addition, when the low-speed internal oscillator is selected, I_{FIL} must be added. When the subsystem clock is running, I_{DD2} contains the operating current of the real time clock.

Note 4: This is the current flowing to the 15-bit interval timer only (excluding the operating current of the low-speed internal oscillator and XT1 oscillator circuit). In the case of 15-bit interval timer operation in run mode or sleep mode, the microcontroller current value is the value of I_{DD1} or I_{DD2} plus I_{IT}. In addition, when selecting the low- speed internal oscillator, I_{FIL} must be added.

Note 5: This is the current flowing to the watchdog timer only (including the operating current of the low-speed internal oscillator). With the watchdog timer running, the microcontroller current value is the value of I_{DD1} or I_{DD2} or I_{DD3} plus I_{WDT}.

Note 6: This is the current flowing to the A/D converter only. In the case of A/D converter operation in run mode or sleep mode, the current value of the microcontroller is the value of I_{DD1} or I_{DD2} plus I_{ADC}.

Note 7: This is the current flowing to the LVD circuit only. In the case of LVD circuit operation, the microcontroller current value is the value of I_{DD1} or I_{DD2} or IDD3 plus I_{LVD}.

Remark:

1. F_{IL}: Clock frequency of the low-speed internal oscillator.
2. The temperature for typical values is T_A = 25°C.
3. Low temperature specification values are guaranteed by design, and low temperature conditions are not measured in mass production.

6.6 AC characteristics

(T_A= -40~85℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition		Min	Typ	Max	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (F_{MAIN}) operation	1.8V≤V_{DD}≤5.5V	0.015625	-	0.5	μs
		Subsystem clock (F_{SUB}) operation	1.8V≤V_{DD}≤5.5V	28.5	30.5	31.3	μs
External system clock frequency	F_{EX}	1.8V≤V_{DD}≤5.5V		4.0	-	16.0	MHz
	F_{EXS}	1.8V≤V_{DD}≤5.5V		32.0	-	35.0	KHz
High and low width of external system clock input	T_{EXH} T_{EXL}	1.8V≤V_{DD}≤5.5V		24	-	-	ns
	T_{EXHS} T_{EXLS}	1.8V≤V_{DD}≤5.5V		13.7	-	-	μs
TI00 ~TI03 TI10 ~TI13 High and low level width of the input	T_{TIH} T_{TIL}	1.8V≤V_{DD}≤5.5V		1/F_{MCK}+10	-	-	ns
TO00 ~ TO03 TO10 ~ TO13 output frequency	F_{TO}	4.0V≤V_{DD}≤5.5V		-	-	16	MHz
		2.4V≤V_{DD}<4.0V		-	-	8	MHz
		1.8V≤V_{DD}<2.4V		-	-	4	MHz
CLKBUZ0 CLKBUZ1 output frequency	F_{PCL}	4.0V≤V_{DD}≤5.5V		-	-	16	MHz
		2.4V≤V_{DD}<4.0V		-	-	8	MHz
		1.8V≤V_{DD}<2.4V		-	-	4	MHz
High and low level width of the interrupt input	T_{INTH} T_{INTL}	INTP0 ~ INTP3	1.8V≤V_{DD}≤5.5V	1	-	-	μs
High and low level width of key interrupt input	T_{KR}	KR0 ~ KR7	1.8V≤V_{DD}≤5.5V	250	-	-	ns
Low level width of RESETB	T_{RSL}	-		10	-	-	μs

Remark:

1. F_{MCK}：Operating clock frequency of Timer4 unit
2. Low temperature specification values are guaranteed by design, and low temperature conditions are not measured in mass production.

6.7 Peripheral function characteristics

6.7.1 General-purpose interface unit

1) UART mode

(T_A= -40~85℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Condition		Specification value		Unit
			Min	Max	
Transfer rate	1.8V ≤ V_{DD} ≤ 5.5V	-	-	F_{MCK}/6	bps
		Theoretical value of the maximum transfer rate F_{MCK}=F_{CLK}	-	10.6	Mbps

Remark: It is guaranteed by design and not tested in mass production.

2) Three-wire SPI mode (master mode, internal clock output)

(T_A= -40~85℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition		-40~85℃		Unit
				Min	Max	
SCLKp cycle time	T_{KCY1}	T_{KCY1} ≥ 2/F_{CLK}	4.0V ≤ V_{DD} ≤ 5.5V	31.25	-	ns
			2.7V ≤ V_{DD} ≤ 5.5V	41.67	-	ns
			2.4V ≤ V_{DD} ≤ 5.5V	65	-	ns
			1.8V ≤ V_{DD} ≤ 5.5V	125	-	ns
SCLKp high/low level width	T_{KH1} T_{KL1}	4.0V ≤ V_{DD} ≤ 5.5V		T_{KCY1}/2-4	-	ns
		2.7V ≤ V_{DD} ≤ 5.5V		T_{KCY1}/2-5	-	ns
		2.4V ≤ V_{DD} ≤ 5.5V		T_{KCY1}/2-10	-	ns
		1.8V ≤ V_{DD} ≤ 5.5V		T_{KCY1}/2-19	-	ns
SDIp set-up time (for SCLKp↑)	T_{SIK1}	4.0V ≤ V_{DD} ≤ 5.5V		12	-	ns
		2.7V ≤ V_{DD} ≤ 5.5V		17	-	ns
		2.4V ≤ V_{DD} ≤ 5.5V		20	-	ns
		1.8V ≤ V_{DD} ≤ 5.5V		28	-	ns
SDIp hold time (for SCLKp↑)	T_{KSI1}	1.8V ≤ V_{DD} ≤ 5.5V		5	-	ns
Delay time from SCLKp↓→ SDOp output	T_{KSO1}	1.8V ≤ V_{DD} ≤ 5.5V C=20pF Note 1		-	5	ns

Note 1: C is the load capacitance of the SCLKp and SDOp output lines.

Notice: Select the SDIp and SCLKp pins as the normal input buffers and the SDOp pin as the normal output mode via the Port Input Mode Register and Port Output Mode Register.

Remark: It is guaranteed by design and not tested in mass production.

3) Three-wire SPI mode (slave mode, external clock input)

(T_A= -40~85℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition		-40~85℃		Unit
				Min	Max	
SCLKp cycle time	T_{KCY2}	4.0V≤V_{DD}≤5.5V	16MHz＜F_{MCK}	8/F_{MCK}	-	ns
			F_{MCK}≤16MHz	6/F_{MCK}	-	ns
		2.7V≤V_{DD}≤5.5V	16MHz＜F_{MCK}	8/F_{MCK}	-	ns
			F_{MCK}≤16MHz	6/F_{MCK}	-	ns
		2.4V≤V_{DD}≤5.5V		6/F_{MCK} and ≥500	-	ns
		1.8V≤V_{DD}≤5.5V		6/F_{MCK} and ≥750	-	ns
SCLKp high/low level width	T_{KH2} T_{KL2}	4.0V≤V_{DD} ≤5.5V		T_{KCY1}/2-7	-	ns
		2.7V≤V_{DD}≤5.5V		T_{KCY1}/2-8	-	ns
		1.8V≤V_{DD}≤5.5V		T_{KCY1}/2-18	-	ns
SDIp set-up time (to SCLKp↑)	T_{SIK2}	2.7V≤V_{DD}≤5.5V		1/F_{MCK}+20	-	ns
		1.8V≤V_{DD}≤5.5V		1/F_{MCK}+30	-	ns
SDIp hold time (for SCLKp↑)	T_{KSI2}	1.8V≤V_{DD}≤5.5V		1/F_{MCK}+31	-	ns
Delay time from SCLKp↓→ SDOp output	T_{KSO2}	2.7V≤V_{DD}≤5.5V C=30pF Note 1		-	2/F_{MCK}+44	ns
		2.4V≤V_{DD}≤5.5V C=30pF Note 1		-	2/F_{MCK}+75	ns
		1.8V≤V_{DD}≤5.5V C=30pF Note 1		-	2/F_{MCK}+100	ns

Note 1: C is the load capacitance of the SCLKp and SDOp output lines.

Notice: Select the SDIp and SCLKp pins as the normal input buffers and the SDOp pin as the normal output mode via the Port Input Mode Register and Port Output Mode Register.

Remark: It is guaranteed by design and not tested in mass production.

4) Four-wire SPI mode (slave mode, external clock input)

(T_A= -40~85℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition		-40~85℃		Unit
				Min	Max	
SSI00 set-up time	T_{SSIK}	DAPmn= 0	2.7V≤V_{DD}≤5.5V	120	-	ns
			1.8V≤V_{DD}≤5.5V	200	-	ns
		DAPmn= 1	2.7V≤V_{DD}≤5.5V	1/F_{MCK}+120	-	ns
			1.8V≤V_{DD}≤5.5V	1/F_{MCK}+200	-	ns
SSI00 hold time	T_{KSSI}	DAPmn= 0	2.7V≤V_{DD}≤5.5V	1/F_{MCK}+120	-	ns
			1.8V≤V_{DD}≤5.5V	1/F_{MCK}+200	-	ns
		DAPmn= 1	2.7V≤V_{DD}≤5.5V	120	-	ns
			1.8V≤V_{DD}≤5.5V	200	-	ns

Notice: Select the SDIp and SCLKp pins as the normal input buffers and the SDOp pin as the normal output mode via the Port Input Mode Register and Port Output Mode Register.

Remark: It is guaranteed by design and not tested in mass production.

6.7.2 Serial interface IICA

1) I²C standard mode

(T_A= -40~85℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition	Specification value		Unit
			Min	Max	
SCLA0 clock frequency	F_{SCL}	Standard mode: F_{CLK}≥1MHz	-	100	KHz
Set-up time of the start condition	$T_{SU:STA}$	-	4.7	-	μs
Hold time of the start condition Note1	$T_{HD:STA}$	-	4.0	-	μs
Hold time when SCLA0 is low	T_{LOW}	-	4.7	-	μs
Hold time when SCLA0 is high	T_{HIGH}	-	4.0	-	μs
Data set-up time (reception)	$T_{SU:DAT}$	-	250	-	ns
Data hold time (transmission) Note2	$T_{HD:DAT}$	-	0	3.45	μs
Set-up time of the stop condition	$T_{SU:STO}$	-	4.0	-	μs
Bus idle time	T_{BUF}	-	4.7	-	μs

Note 1: Generates the first clock pulse after a start condition or a restart condition is generated.

Note 2: The maximum (MAX.) value of $T_{HD:DAT}$ needs to be guaranteed during normal transmission and needs to be waited during acknowledger (ACK).

Notice: The maximum value of C_b (communication line capacitance) for each mode and the value of R_b (pull-up resistor value of the communication line) at this time are as follows:

Standard mode: C_b=400pF, R_b=2.7kΩ

Remark: It is guaranteed by design and not tested in mass production.

2) I²C fast mode

(T_A= -40~85℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition	Specification value		Unit
			Min	Max	
SCLA0 clock frequency	F_{SCL}	Fast mode: F_{CLK}≥3.5MHz	-	400	KHz
Set-up time of the start condition	$T_{SU:STA}$	-	0.6	-	μs
Hold time of the start condition Note1	$T_{HD:STA}$	-	0.6	-	μs
Hold time when SCLA0 is low	T_{LOW}	-	1.3	-	μs
Hold time when SCLA0 is high	T_{HIGH}	-	0.6	-	μs
Data set-up time (reception)	$T_{SU:DAT}$	-	100	-	ns
Data hold time (transmission) Note2	$T_{HD:DAT}$	-	0	0.9	μs
Set-up time of the stop condition	$T_{SU:STO}$	-	0.6	-	μs
Bus idle time	T_{BUF}	-	1.3	-	μs

Note 1: Generates the first clock pulse after a start condition or a restart condition is generated.

Note 2: The maximum (MAX.) value of $T_{HD:\ DAT}$ needs to be guaranteed during normal transmission and needs to be waited during acknowledger (ACK).

Notice: The maximum value of C_b (communication line capacitance) for each mode and the value of R_b (pull-up resistor value of the communication line) at this time are as follows:

Fast mode: C_b=320pF, R_b=1.1KΩ

Remark: It is guaranteed by design and not tested in mass production.

3) I²C Enhanced fast mode

(T_A= -40~85℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition	Specification value		Unit
			Min	Max	
SCLA0 clock frequency	F_{SCL}	Enhanced fast mode: F_{CLK}≥10MHz	-	1000	KHz
Set-up time of the start condition	$T_{SU:STA}$	-	0.26	-	μs
Hold time of the start condition Note1	$T_{HD:STA}$	-	0.26	-	μs
Hold time when SCLA0 is low	T_{LOW}	-	0.5	-	μs
Hold time when SCLA0 is high	T_{HIGH}	-	0.26	-	μs
Data set-up time (reception)	$T_{SU:DAT}$	-	50	-	ns
Data hold time (transmission) Note2	$T_{HD:DAT}$	-	0	0.45	μs
Set-up time of the stop condition	$T_{SU:STO}$	-	0.26	-	μs
Bus idle time	T_{BUF}	-	0.5	-	μs

Note 1: Generates the first clock pulse after a start condition or restart condition is generated.

Note 2: The maximum (MAX.) value of $T_{HD:DAT}$ needs to be guaranteed during normal transmission and needs to be waited during acknowledger (ACK).

Notice: The maximum value of C_b (communication line capacitance) for each mode and the value of R_b (pull-up resistor value of the communication line) at this time are as follows:

Enhanced fast mode: C_b=120pF, R_b=1.1KΩ

Remark: It is guaranteed by design and not tested in mass production.

6.8 Analog characteristics

6.8.1 A/D converter characteristics

Classification of A/D converter characteristics

Input channel \ Reference Voltage	Reference voltage (+) = V_{DD} Reference voltage (-) = V_{SS}
ANI0~ANI19	Refer to the table below
Internal reference voltage Temperature sensor output voltage	

1) When reference voltage(+)=V_{DD}, reference voltage(-)=V_{SS}

(T_A= -40~85℃, 3.0V≤V_{DD}≤5.5V, V_{SS}=0V, reference voltage(+)=V_{DD}, reference voltage(-)=V_{SS})

Item	Symbol	Condition		Min	Typ	Max	Unit
Resolution	RES			-	12	-	bit
Overall error Note 1	AINL	12-bit resolution	3.0V≤V_{DD}≤5.5V	-	6	-	LSB
Conversion time Note3	T_{CONV}	12-bit resolution Target pin: ANI0~ANI19	3.0V≤V_{DD}≤5.5V	16	-	-	Tmclk
Zero-scale error Note1	E_{ZS}	12-bit resolution	3.0V≤V_{DD}≤5.5V	-	0	-	LSB
Full-scale error Note 1	E_{FS}	12-bit resolution	3.0V≤V_{DD}≤5.5V	-	0	-	LSB
Integral linearity error Note 1	ILE	12-bit resolution	3.0V≤V_{DD}≤5.5V	-	-	±4	LSB
Differential linearity error Note 1	DLE	12-bit resolution	3.0V≤V_{DD}≤5.5V	-	-	±3	LSB
Analog input voltage	V_{AIN}	ANI0~ANI19		0	-	V_{DD}	V
		Internal reference voltage (3.0V≤V_{DD}≤5.5V)		V_{BGR} Note 2			V
		Temperature sensor output voltage (3.0V≤V_{DD}≤5.5V)		V_{TMPS25} Note 2			V

Note 1: Excludes quantization error (±1/2 LSB).

Note 2: Refer to “6.8.2 Characteristics of temperature sensor/internal reference voltage”.

Note 3: T_{MCLK} is the action clock period of AD, and the maximum action frequency is 8MHz.

Remark: It is guaranteed by design and not tested in mass production.

6.8.2 Characteristics of temperature sensor/internal reference voltage

(T_A= -40~85℃, 3.0V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition	Min	Typ	Max	Unit
Temperature sensor output voltage	V_{TMPS25}	ADS register=80H, T_A=25℃	-	1.09	-	V
Internal reference voltage	V_{BGR}	ADS register=81H	1.38	1.45	1.5	V
Temperature coefficient	F_{VTMPS}	-	-	-3.5	-	mV/℃
Operation stabilization wait time	T_{AMP}	-	5	-	-	μs

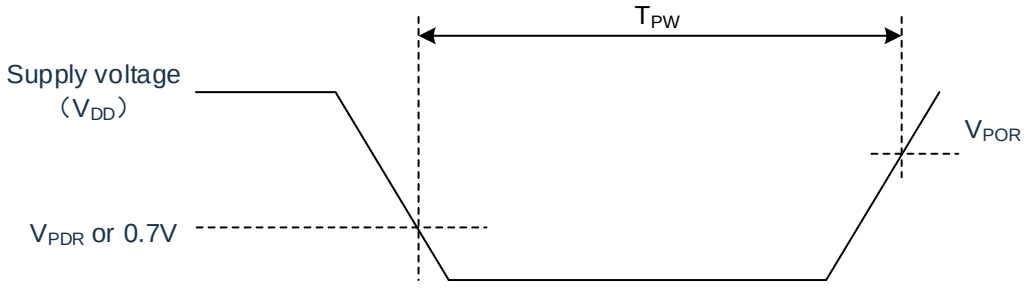
Remark: Low temperature specification values are guaranteed by design, and low temperature conditions are not measured in mass production.

6.8.3 POR circuit characteristics

(T_A= -40~85℃, V_{SS}=0V)

Item	Symbol	Condition	Min	Typ	Max	Unit
Detection voltage	V_{POR}	The power supply voltage is rising	-	1.50	1.75	V
	V_{PDR}	The power supply voltage is falling	1.37	1.45	-	V
Minimum pulse width Note 1	T_{PW}	-	300	-	-	μs

Note 1: Minimum time required for a POR reset when V_{DD} exceeds below V_{PDR}. This is also the minimum time required for a POR reset from when VDD exceeds below 0.7 V to when VDD exceeds VPOR while deep sleep mode is entered or the main system (F_{MAIN}) clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



Remark: It is guaranteed by design and not tested in mass production.

6.8.4 LVD circuit characteristics

1. Reset mode, interrupt mode

(T_A= -40~85℃, V_{PDR}≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition	Min	Typ	Max	Unit
Detection voltage	V_{LVD0}	The power supply voltage is rising.	-	4.06	4.14	V
		The power supply voltage is falling.	3.90	3.98	-	V
	V_{LVD1}	The power supply voltage is rising.	-	3.75	-	V
		The power supply voltage is falling.	-	3.67	-	V
	V_{LVD2}	The power supply voltage is rising.	-	3.13	-	V
		The power supply voltage is falling.	-	3.06	-	V
	V_{LVD3}	The power supply voltage is rising.	-	3.02	-	V
		The power supply voltage is falling.	-	2.96	-	V
	V_{LVD4}	The power supply voltage is rising.	-	2.92	-	V
		The power supply voltage is falling.	-	2.86	-	V
	V_{LVD5}	The power supply voltage is rising.	-	2.81	-	V
		The power supply voltage is falling.	-	2.75	-	V
	V_{LVD6}	The power supply voltage is rising.	-	2.71	-	V
		The power supply voltage is falling.	-	2.65	-	V
	V_{LVD7}	The power supply voltage is rising.	-	2.61	-	V
		The power supply voltage is falling.	-	2.55	-	V
	V_{LVD8}	The power supply voltage is rising.	-	2.50	-	V
		The power supply voltage is falling.	-	2.45	-	V
	V_{LVD9}	The power supply voltage is rising.	-	2.09	-	V
		The power supply voltage is falling.	-	2.04	-	V
	V_{LVD10}	The power supply voltage is rising.	-	1.98	-	V
		The power supply voltage is falling.	-	1.94	-	V
	V_{LVD11}	The power supply voltage is rising.	-	1.88	1.91	V
		The power supply voltage is falling.	1.80	1.84	-	V
Minimum	T_{LW}	-	300	-	-	μs

pulse width						
Detection delay time	-	-	-	-	300	μs

Remark: It is guaranteed by design and not tested in mass production.

2. Interrupt & Reset mode

(T_A= -40~85℃, V_{PDR}≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition			Min	Typ	Max	Unit
Interrupt & Reset mode	V_{LVDA0}	V_{POC2}=0 V_{POC1}=0 V_{POC0}=0	Falling reset voltage		1.60	1.63	-	V
	V_{LVDA1}		LVIS1=1 LVIS0=0	Rising release reset voltage	-	1.77	1.81	V
				Falling interrupt voltage	1.70	1.73	-	V
	V_{LVDA2}		LVIS1=0 LVIS0=1	Rising release reset voltage	-	1.88	-	V
				Falling interrupt voltage	-	1.84	-	V
	V_{LVDA3}		LVIS1=0 LVIS0=0	Rising release reset voltage	-	2.92	-	V
				Falling interrupt voltage	-	2.86	-	V
	V_{LVDB0}	V_{POC2}=0 V_{POC1}=0 V_{POC0}=1	Falling reset voltage			1.84	-	V
	V_{LVDB1}		LVIS1=1 LVIS0=0	Rising release reset voltage	-	1.98	-	V
				Falling interrupt voltage	-	1.94	-	V
	V_{LVDB2}		LVIS1=0 LVIS0=1	Rising release reset voltage	-	2.09	-	V
				Falling interrupt voltage	-	2.04	-	V
	V_{LVDB3}		LVIS1=0 LVIS0=0	Rising release reset voltage	-	3.13	-	V
				Falling interrupt voltage	-	3.06	-	V
	V_{LVDC0}	V_{POC2}=0 V_{POC1}=1 V_{POC0}=0	Falling reset voltage			2.45	-	V
	V_{LVDC1}		LVIS1=1 LVIS0=0	Rising release reset voltage	-	2.61	-	V
				Falling interrupt voltage	-	2.55	-	V
	V_{LVDC2}		LVIS1=0 LVIS0=1	Rising release reset voltage	-	2.71	-	V
				Falling interrupt voltage	-	2.65	-	V
	V_{LVDC3}		LVIS1=0 LVIS0=0	Rising release reset voltage	-	3.75	-	V
				Falling interrupt voltage	-	3.67	-	V
	V_{LVDD0}	V_{POC2}=0 V_{POC1}=1 V_{POC0}=1	Falling reset voltage		-	2.75	-	V
	V_{LVDD1}		LVIS1=1 LVIS0=0	Rising release reset voltage	-	2.92	-	V
				Falling interrupt voltage	-	2.86	-	V
	V_{LVDD2}		LVIS1=0 LVIS0=1	Rising release reset voltage	-	3.02	-	V
				Falling interrupt voltage	-	2.96	-	V
	V_{LVDD3}		LVIS1=0 LVIS0=0	Rising release reset voltage	-	4.06	4.14	V
				Falling interrupt voltage	3.90	3.98	-	V

Remark: It is guaranteed by design and not tested in mass production.

6.8.5 Power supply voltage rising slope characteristics

(T_A= -40~85℃, V_{SS}=0V)

Item	Symbol	Condition	Min	Typ	Max	Unit
Power supply voltage rising slope	S_{VDD}	-	-	-	54	V/ms

Remark: It is guaranteed by design and not tested in mass production.

6.9 Memory characteristics

6.9.1 Flash memory

(T_A= -40~85℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Symbol	Item	Condition	Min	Max	Unit
T_{PROG}	Word write time (32bit)	T_A= -40~85℃	-	120	μs
T_{ERASE}	Sector erase time (512B)	T_A= -40~85℃	2	3	ms
	Chip erase time	T_A= -40~85℃	30	40	ms
N_{END}	Number of rewritable times	T_A= -40~85℃	100	-	k cycle
T_{RET}	Data retention period	100k cycles Note 1 at TA =85℃	20	-	Years

Note 1: Cycling tests are performed within the temperature range.

Remark: It is guaranteed by design and not tested in mass production.

6.9.2 RAM memory

(T_A= -40~85℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Symbol	Item	Condition	Min	Max	Unit
$V_{RAMHOLD}$	RAM hold voltage	T_A= -40~85℃	0.8	-	V

Remark: It is guaranteed by design and not tested in mass production.

6.10 EMS characteristics

6.10.1 ESD electrical characteristics

Symbol	Item	Test conditions	Grade
$V_{ESD(HBM)}$	Electrostatic discharge (Human-Body Model HBM)	T_A = 25℃, JESD22-A114	3A

Remark: It is guaranteed by design and not tested in mass production.

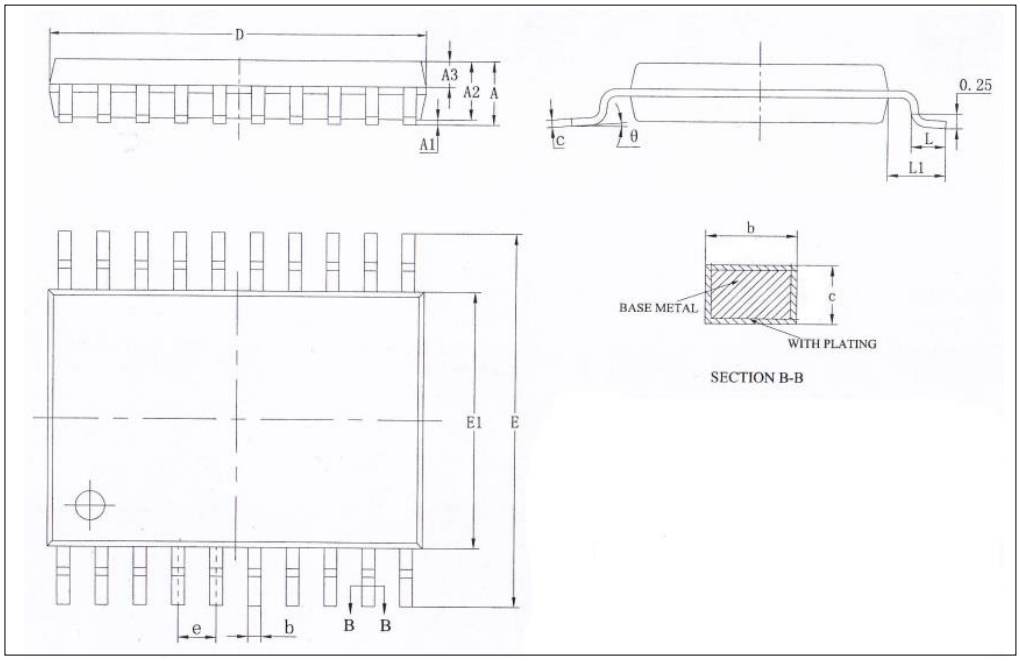
6.10.2 Latch-up electrical characteristics

Symbol	Item	Test conditions	Classification
LU	Static latch-up class	T_A = 25℃, JESD78F	I levelA

Remark: It is guaranteed by design and not tested in mass production.

7 Package Information

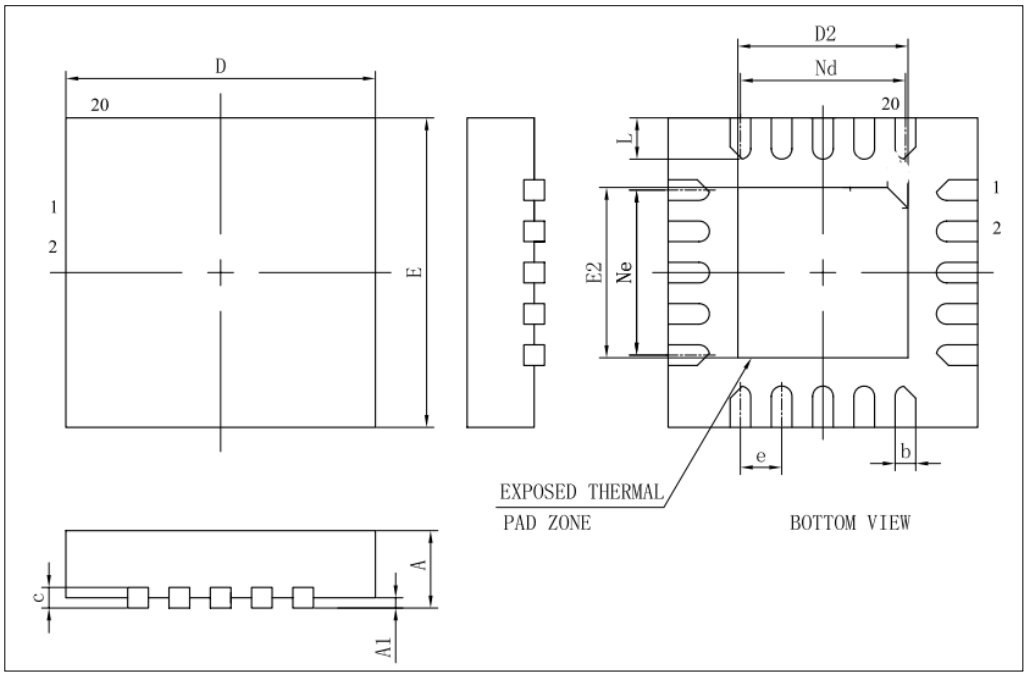
7.1 TSSOP20



Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.25
A1	0.05	-	0.15
A2	0.80	1.00	1.10
A3	0.34	0.44	0.54
b	0.20	-	0.28
c	0.10	-	0.19
D	6.40	6.50	6.60
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ	0	-	8°

Caution: Package dimensions do not include mold flash or gate burrs.

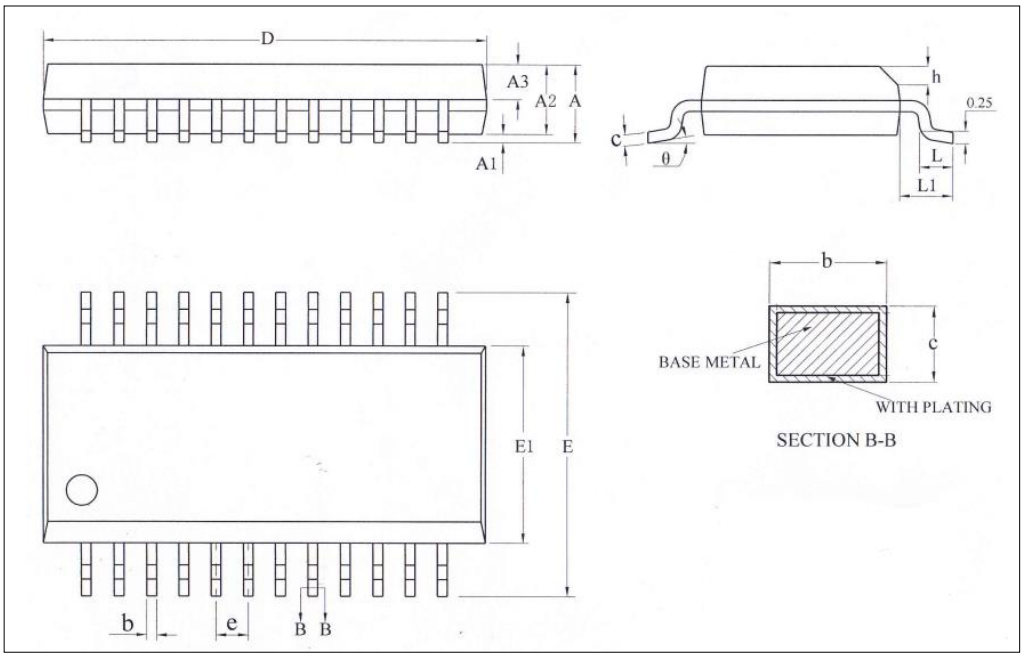
7.2 QFN20（3x3x0.75-0.40mm）



Symbol	Millimeter		
	Min	Nom	Max
A	0.65	0.75	0.85
A1	-	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	2.90	3.00	3.10
D2	1.55	-	2.00
e	0.40BSC		
Ne	1.60BSC		
Nd	1.60BSC		
E	2.90	3.00	3.10
E2	1.55	-	2.00
L	0.20	-	0.50

Caution: Package dimensions do not include mold flash or gate burrs.

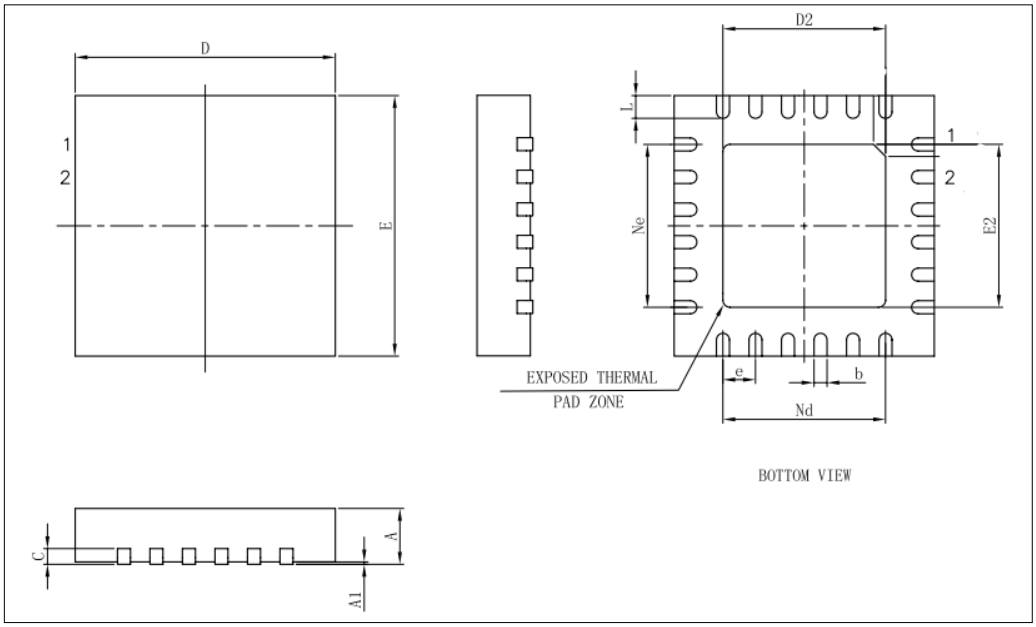
7.3 SSOP24（0.635mm）



Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.80
A1	0.10	0.15	0.25
A2	1.30	-	1.55
A3	0.60	0.65	0.70
b	0.20	-	0.31
c	0.20	-	0.24
D	8.53	-	8.75
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	0.635BSC		
h	0.30	-	0.50
L	0.406	-	0.889
L1	1.05REF		
θ	0	-	8°

Caution: Package dimensions do not include mold flash or gate burrs.

7.4 QFN24（4x4x0.75-0.50mm）



Symbol	Millimeter		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	-	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.20	-	2.80
e	0.50BSC		
Ne	2.50BSC		
Nd	2.50BSC		
E	3.90	4.00	4.10
E2	2.20	-	2.80
L	0.30	0.40	0.50
h	0.25	-	0.40

Caution: Package dimensions do not include mold flash or gate burrs.

8 Revision History

Version	Date	Revised content
V1.0.0	June 2023	Initial version
V1.0.1	June 2023	1. Correct 5.7incorrect content 2. Change the product name from “CMS32L032GExx” to “CMS32L032DExx” 3. Modify product selection table parameters
V1.0.2	August 2023	1. Remove the Features section on simplified I^2C 2. Modify the Product Block Diagram 3. Delete section 5.16.4 Simplified I2C 4. Correct the data length in sections 5.16.1, 5.16.2, 5.16.3 5. Removed the description of the WDTE register execution of bit operation instruction in the 5.10 Watchdog Timers section 6. Remove the simplified IIC mode in the 6.7.1 general-purpose interface unit
V1.0.3	Oct 2023	Corrected QFN24 pin map
V1.0.4	Mar 2024	Modified power consumption in deep sleep mode with partial power down in section Function/1.1/6.5.2
V1.0.5	Apr 2024	Modified section 6.1 Typical application peripheral circuits
V1.0.6	Jun 2024	Modified section 4.1 Port function
V1.0.7	Sep 2024	1. Revised the cover page 2. Modifying EMS Features 3. Modified TSSOP20/QFN20/SSOP24/QFN24 package dimensions
V1.0.8	Dec 2024	Modified IO port high/low level input voltage parameters in Section 6.5.1